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**Customer :**

**Part Name: Y1111-EB**

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Seoul Viosys Co., Ltd.		
Drawn by	Checked by	Approved by
김재권	김종규	채종현
15/11/10	15/11/10	15/11/10

Seoul Semiconductor Co., Ltd.		
	Checked by	Approved by

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**1. Features and Application**

- High Luminous Intensity, Long Operation Life
- Package-less module

**2. Part Name:**

- Y1111-EB

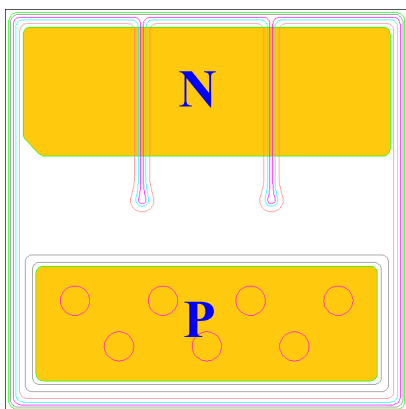
**3. Main Material**

- Substrate: Al<sub>2</sub>O<sub>3</sub> (Sapphire)
- Epitaxial Layer: GaN Based LED Structure

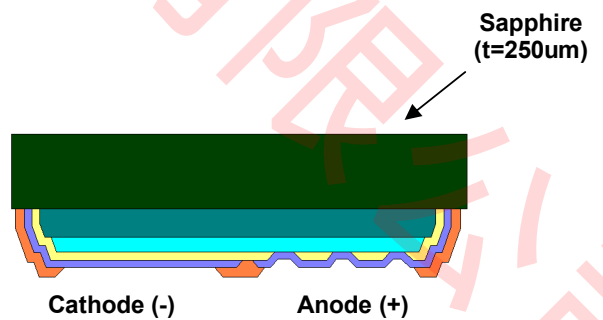
**4. Electrodes**

- P-Electrode: Au alloy
- N-Electrode: Au alloy

**5. Chip Diagram**



<Fig. 1 >Plane View



<Fig. 2 > Cross Sectional View

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Item	Symbol	Value	Unit
<b>DC forward current (Ta=25°C)</b>	$I_f$	800	mA
<b>Pulsed forward current <sup>a</sup> (Ta=25°C)</b>	$I_{fp}$	1000	mA
<b>Junction temperature <sup>b</sup></b>	$T_j$	125	°C
<b>Operating Temperature Range</b>	$T_{op}$	-30 to + 85	°C
<b>Storage Temperature Range</b>	$T_{st}$	-40 to +100	°C

## 6. Maximum Ratings

Note. 'Maximum Ratings' mean when it exceeds the chip has the possibility of breaking down when these conditions are exceeded momentarily. 'Maximum ratings', the chip is not guaranteed to endure such conditions. 'Maximum Ratings' concerning your LED device after the chip is built into your package shall be established by yourself since these greatly depend on the design of the device, the conditions of assembly, the environment used, and so forth.

<sup>a</sup> 1/10 Duty , f=1kHz

<sup>b</sup> Measurement condition ; Metal Core PCB

## 7. Typical Electro-Optical Characteristics at Ta=25°C

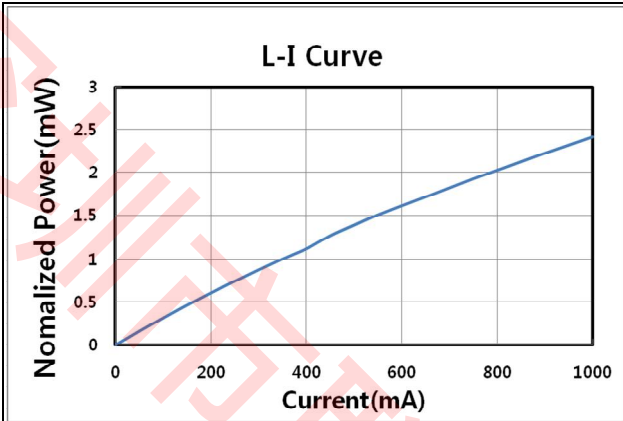
Item	Symbol	Condition	Characteristics (Ta=25°C)			Unit
			Min	Typ	Max	
<b>Reverse Current</b>	$I_R$	$V_R = -5V$	0	-	1.0	uA
<b>Turn-on Voltage</b>	$V_{F1}$	$I_F = 1 \mu A$	1.9	-	2.8	V
<b>Forward Voltage</b>	$V_F$	$I_F = 350mA$	2.8	3.05	3.25	V
<b>Dominant Wavelength <sup>1)</sup></b>	$\lambda_d$	$I_F = 350mA$	445.0	-	460.0	nm
<b>Full Width Half Maximum</b>	$\Delta\lambda$	$I_F = 350mA$	-	30	-	nm
<b>Radiant Power <sup>2)</sup></b>	$P_o$	$I_F = 350mA$	450	475	530	mW

Note: Radiant and Peak wavelength are measured by Seoul Viosys' equipment. (\*1, \*2)

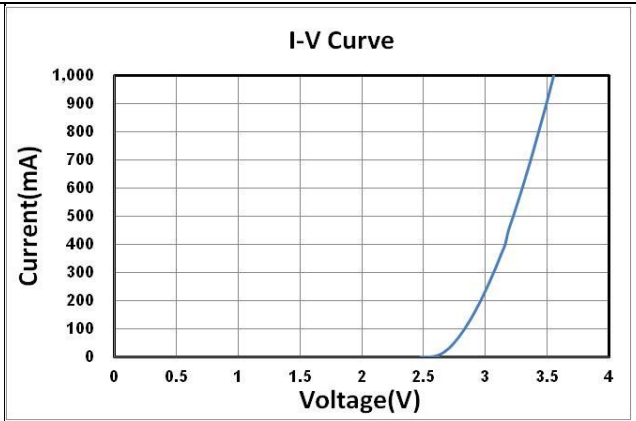
Dominant Wavelength:  $\pm 1nm$ . (\*1)

Radiant Power :  $\pm 10\%$ . (\*2)

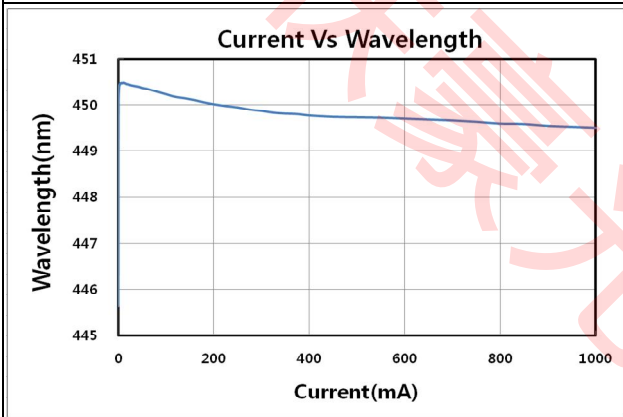
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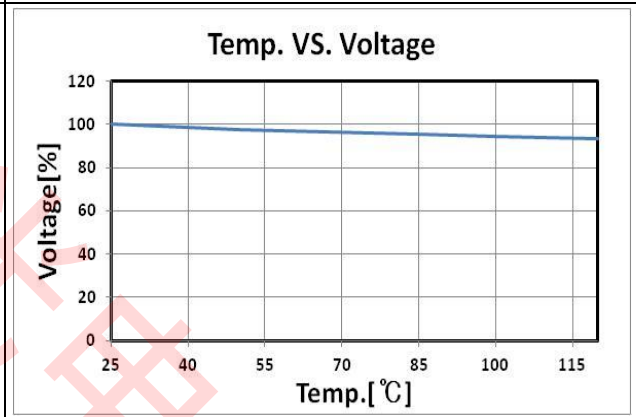
Forward Current vs. Light Output



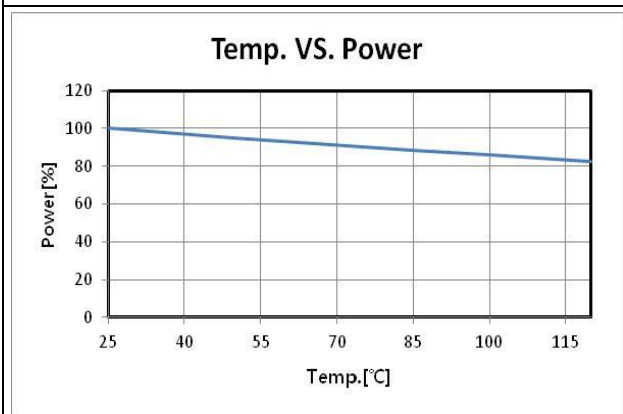
Forward Voltage vs. Forward Current



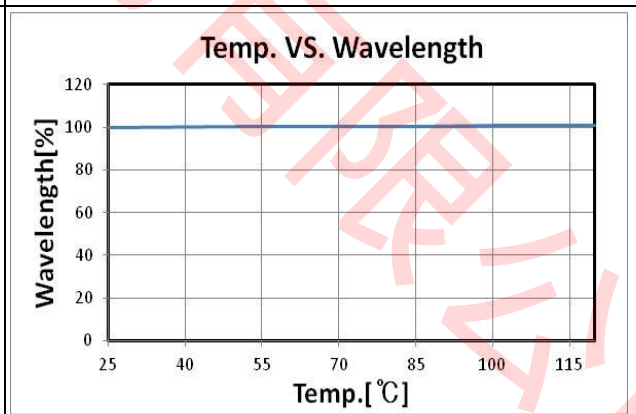
Forward Current vs. Wavelength



Temperature vs. Relative Forward Voltage



Temperature vs. Relative Light Output



Temperature vs. Relative Wavelength

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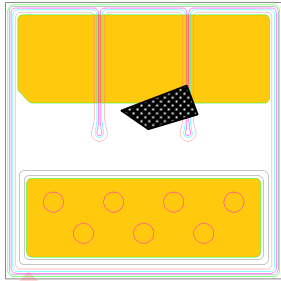
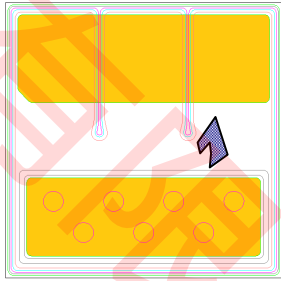
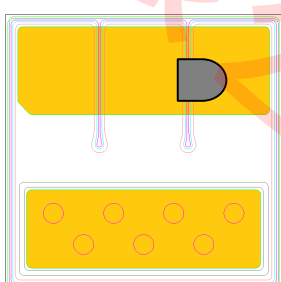
### 8. Mechanical Specifications

(Unit:  $\mu\text{m}$ )

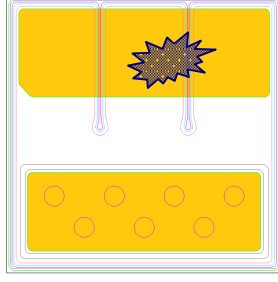
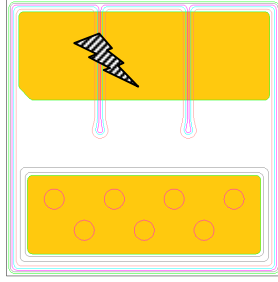
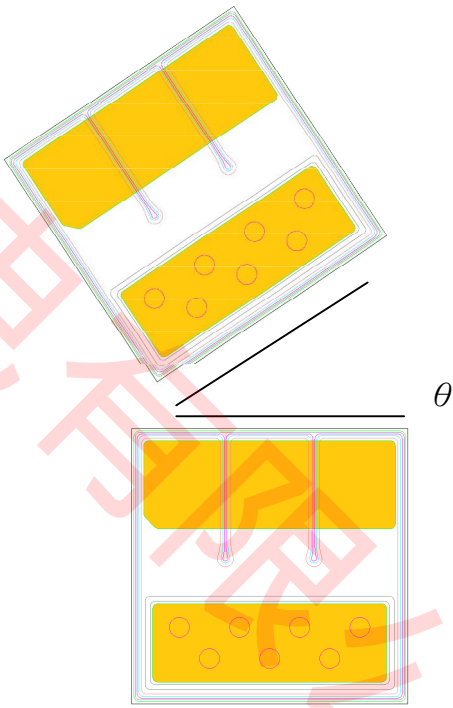
Description	Dimension	Tolerance
Top emitting area	1100 $\mu\text{m}$ x 1100 $\mu\text{m}$	$\pm 40$
Bottom substrate	1100 $\mu\text{m}$ x 1100 $\mu\text{m}$	$\pm 40$
Chip Thickness	250 $\mu\text{m}$	$\pm 15$
P-Pad Diameter	932 $\mu\text{m}$ x 313 $\mu\text{m}$	$\pm 50$
N-Pad Diameter	1002 $\mu\text{m}$ x 351 $\mu\text{m}$	$\pm 50$

### 9. Visual inspection

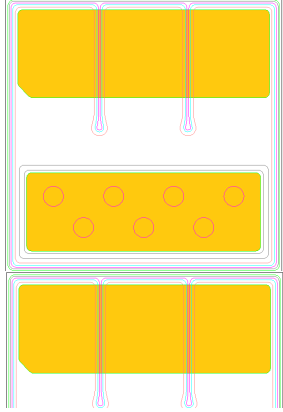
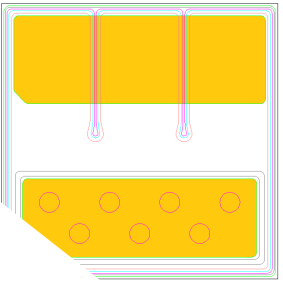
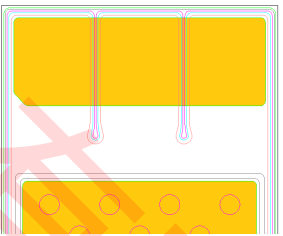
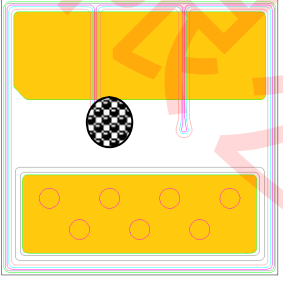
Done by optical microscope (20x).

Item	Accepted (OK)/defective (N.G.)	Example
Surface dirt	accepted : if surface dirt(metal) less than 20% of chip	
Passivation film peeling	accepted : if Passivation film peeling less than 30% of chip.	
Partially missing pad	accepted : $a < b/5$ a: missing bond pad b: normal bond pad	

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Metal peeling	rejected : if Metal peeling more than 20% of chip area.	
Bond pad scratch	accepted : if bond pad scratch ( including probe mark) less than 20 % of chip area.	
$\theta$ shift	accepted : $\theta < \pm 5^\circ$	

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Twins or triples	Inseparable chips are rejected If extra-size is less than 10%, OK.	
Chipping	Pad electrode not chipped off	
Bad cut	Not accepted : if bad cut is occurred	
Pinholes	accepted : if pinhole less than 20% of chip	

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**10. Sorting Bins and Product name**

제품명	BIN	Reverse Leakage @-5V	Forward Voltage(V) @1uA	Forward Voltage(V) @ 350mA	Power(mW) @ 350mA	Wave Length(nm) @ 350mA
Y1111-EB-W01	1	0~1	1.9~2.8	2.8~3.1	460~470	445~447.5
Y1111-EB-W02	2	0~1	1.9~2.8	2.8~3.1	470~480	445~447.5
Y1111-EB-W03	3	0~1	1.9~2.8	2.8~3.1	480~490	445~447.5
Y1111-EB-W04	4	0~1	1.9~2.8	2.8~3.1	490~510	445~447.5
Y1111-EB-W05	5	0~1	1.9~2.8	2.8~3.1	510~530	445~447.5
Y1111-EB-W06	6	0~1	1.9~2.8	3.1~3.25	460~470	445~447.5
Y1111-EB-W07	7	0~1	1.9~2.8	3.1~3.25	470~480	445~447.5
Y1111-EB-W08	8	0~1	1.9~2.8	3.1~3.25	480~490	445~447.5
Y1111-EB-W09	9	0~1	1.9~2.8	3.1~3.25	490~510	445~447.5
Y1111-EB-W10	10	0~1	1.9~2.8	3.1~3.25	510~530	445~447.5
Y1111-EB-X01	11	0~1	1.9~2.8	2.8~3.1	460~470	447.5~450
Y1111-EB-X02	12	0~1	1.9~2.8	2.8~3.1	470~480	447.5~450
Y1111-EB-X03	13	0~1	1.9~2.8	2.8~3.1	480~490	447.5~450
Y1111-EB-X04	14	0~1	1.9~2.8	2.8~3.1	490~510	447.5~450
Y1111-EB-X05	15	0~1	1.9~2.8	2.8~3.1	510~530	447.5~450
Y1111-EB-X06	16	0~1	1.9~2.8	3.1~3.25	460~470	447.5~450
Y1111-EB-X07	17	0~1	1.9~2.8	3.1~3.25	470~480	447.5~450
Y1111-EB-X08	18	0~1	1.9~2.8	3.1~3.25	480~490	447.5~450
Y1111-EB-X09	19	0~1	1.9~2.8	3.1~3.25	490~510	447.5~450
Y1111-EB-X10	20	0~1	1.9~2.8	3.1~3.25	510~530	447.5~450
Y1111-EB-Y01	21	0~1	1.9~2.8	2.8~3.1	460~470	450~452.5
Y1111-EB-Y02	22	0~1	1.9~2.8	2.8~3.1	470~480	450~452.5
Y1111-EB-Y03	23	0~1	1.9~2.8	2.8~3.1	480~490	450~452.5
Y1111-EB-Y04	24	0~1	1.9~2.8	2.8~3.1	490~510	450~452.5
Y1111-EB-Y05	25	0~1	1.9~2.8	2.8~3.1	510~530	450~452.5
Y1111-EB-Y06	26	0~1	1.9~2.8	3.1~3.25	460~470	450~452.5
Y1111-EB-Y07	27	0~1	1.9~2.8	3.1~3.25	470~480	450~452.5
Y1111-EB-Y08	28	0~1	1.9~2.8	3.1~3.25	480~490	450~452.5
Y1111-EB-Y09	29	0~1	1.9~2.8	3.1~3.25	490~510	450~452.5
Y1111-EB-Y10	30	0~1	1.9~2.8	3.1~3.25	510~530	450~452.5



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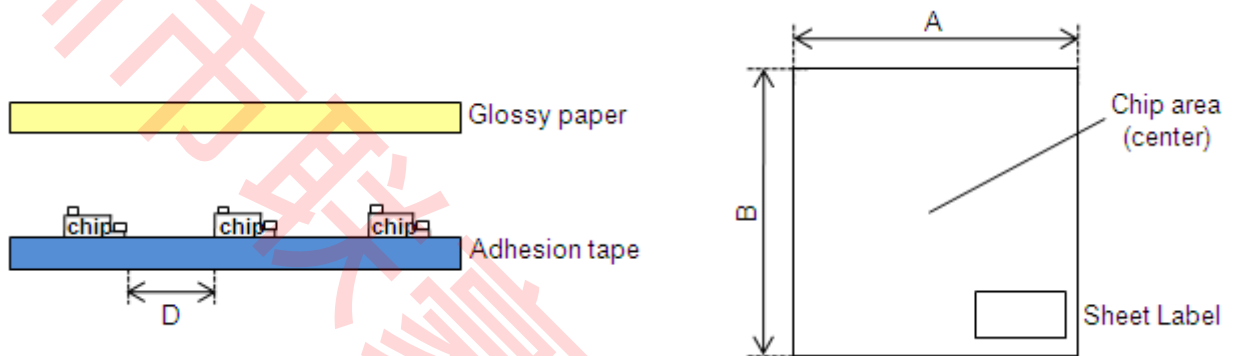
Y1111-EB-Z01	31	0~1	1.9~2.8	2.8~3.1	460~470	452.5~455
Y1111-EB-Z02	32	0~1	1.9~2.8	2.8~3.1	470~480	452.5~455
Y1111-EB-Z03	33	0~1	1.9~2.8	2.8~3.1	480~490	452.5~455
Y1111-EB-Z04	34	0~1	1.9~2.8	2.8~3.1	490~510	452.5~455
Y1111-EB-Z05	35	0~1	1.9~2.8	2.8~3.1	510~530	452.5~455
Y1111-EB-Z06	36	0~1	1.9~2.8	3.1~3.25	460~470	452.5~455
Y1111-EB-Z07	37	0~1	1.9~2.8	3.1~3.25	470~480	452.5~455
Y1111-EB-Z08	38	0~1	1.9~2.8	3.1~3.25	480~490	452.5~455
Y1111-EB-Z09	39	0~1	1.9~2.8	3.1~3.25	490~510	452.5~455
Y1111-EB-Z10	40	0~1	1.9~2.8	3.1~3.25	510~530	452.5~455
Y1111-EB-A01	41	0~1	1.9~2.8	2.8~3.1	450~460	455~457.5
Y1111-EB-A02	42	0~1	1.9~2.8	2.8~3.1	460~470	455~457.5
Y1111-EB-A03	43	0~1	1.9~2.8	2.8~3.1	470~480	455~457.5
Y1111-EB-A04	44	0~1	1.9~2.8	2.8~3.1	480~500	455~457.5
Y1111-EB-A05	45	0~1	1.9~2.8	2.8~3.1	500~520	455~457.5
Y1111-EB-A06	46	0~1	1.9~2.8	3.1~3.25	450~460	455~457.5
Y1111-EB-A07	47	0~1	1.9~2.8	3.1~3.25	460~470	455~457.5
Y1111-EB-A08	48	0~1	1.9~2.8	3.1~3.25	470~480	455~457.5
Y1111-EB-A09	49	0~1	1.9~2.8	3.1~3.25	480~500	455~457.5
Y1111-EB-A10	50	0~1	1.9~2.8	3.1~3.25	500~520	455~457.5
Y1111-EB-B01	51	0~1	1.9~2.8	2.8~3.1	450~460	457.5~460
Y1111-EB-B02	52	0~1	1.9~2.8	2.8~3.1	460~470	457.5~460
Y1111-EB-B03	53	0~1	1.9~2.8	2.8~3.1	470~480	457.5~460
Y1111-EB-B04	54	0~1	1.9~2.8	2.8~3.1	480~500	457.5~460
Y1111-EB-B05	55	0~1	1.9~2.8	2.8~3.1	500~520	457.5~460
Y1111-EB-B06	56	0~1	1.9~2.8	3.1~3.25	450~460	457.5~460
Y1111-EB-B07	57	0~1	1.9~2.8	3.1~3.25	460~470	457.5~460
Y1111-EB-B08	58	0~1	1.9~2.8	3.1~3.25	470~480	457.5~460
Y1111-EB-B09	59	0~1	1.9~2.8	3.1~3.25	480~500	457.5~460
Y1111-EB-B10	60	0~1	1.9~2.8	3.1~3.25	500~520	457.5~460

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### 11. Packing

(1) Chips on tape

- (a) Electro-Optical measurement data should be labeled and tacked on the backside of the glossy paper. Chip area should be placed in the center of adhesion tape, and the wire-bonding pad should face towards the covered glossy paper.



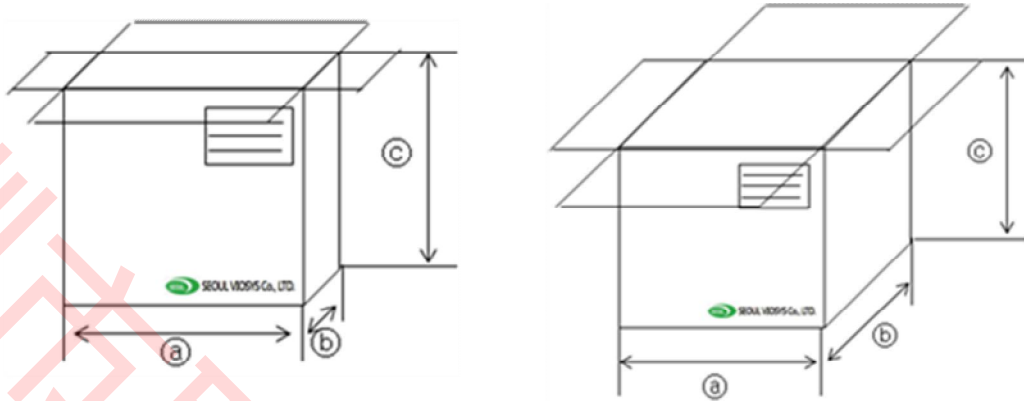
- (b) Chip type, Lot No. and quantity etc. should be labeled and tacked to the corner of the glossy paper.

Item	Instruction
Adhesion tape	Semi- transparent blue
Glossy paper (A×B)	197mm × 220mm
Chip Qty tape	Typ. 2,000ea
Chip separation (D)	D : 0.40mm

(2) Packing for shipment

- (a) The sheets (adhesion tape + glossy paper) are packed in an anti-static electricity bag. Each anti-static bag can contain up to 20 sheets.
- (b) The anti-static bags are packed in a box. The size of this box is 250mm×65mm×275mm (a × b × c). Each box can contain up to 5 anti-static electricity bags.
- (c) The boxes which contain anti-static electricity bags are packed in the other box. The size of this outer box is 260mm×340mm×290mm (a × b × c). Each outer box can contain up to 5 inner boxes.
- (d) Each sheet / box is labeled with information describing its content. (Details please refer to section 12)

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## 12. Labeling

Sheet	Inner Box	Outer Box
		

- (1) Sheet : The measurement data for each lot are also shown on the backside of the sheet.
- (2) Inner Box : The information about the products is also shown on the inner box.
- (3) Outer Box : The information about the products is also shown on the outer box.

## 13. Precaution

### (1) Quality Guarantee

The chip guarantee period is three months after the delivery under the following preservation conditions. If any defective is found, the customer shall immediately inform of that to Seoul Viosys Co., Ltd. Preservation conditions (when the shipping package is unopened.)

- Temperature: 0 ~ 60 °C
- Atmosphere: Keep the chips in a desiccator with silica gel or with nitrogen substitution.

### (2) General precautions for use

- Chips should be stored in a clean environment. If the Chips are to be stored for 3 months or more after being shipped from Seoul Viosys, they should be packed by a sealed

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container with nitrogen gas injected.

(Shelf life of sealed bags : 1year, 0~40°C of temperature , 20~70% of RH)

· This chip should not be used directly in any type of fluid such as water, oil, organic solvent, etc. When washing is required, IPA is recommended to use.

· After storage bag is open, device subjected to soldering, solder flow, or other high temperature processes must be:

Mounted within 168 hours (7days) at an assembly line with a condition of no more than 30°C and 60% RH

· Chips require baking before mounting, if humidity card reading is >60% at, 23.5°C. chips must be baked for 24Hrs. at 65.5°C, if baking required.

· When the chips are illuminating, the maximum ambient temperature should be first considered before operation. If voltage exceeding the absolute maximum rating is applied to chips, it may cause damage or even destruction to chips. Damaged LEDs will show some abnormal characteristics such as remarkable increase of leak current, lower turn-on voltage and getting unlit at low current.

· The appearance and specifications of the products may be modified for improvement without further notice.

· The chips are sensitive to the static electricity and surge. It is strongly recommended to use a grounded wrist band and anti-electrostatic glove when handling the LEDs.

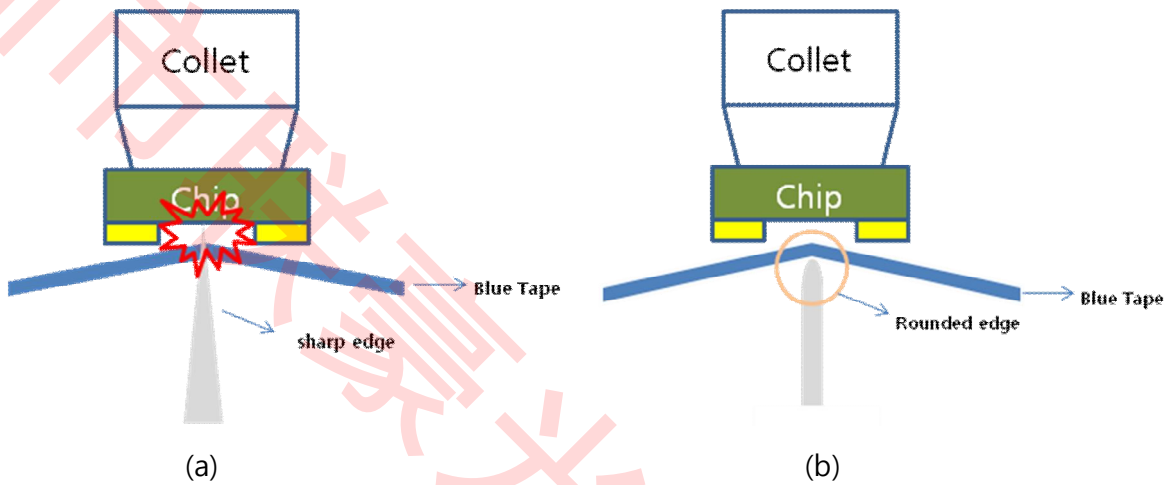
### (3) Precautions for Die Attach (Pick and Place)

· Unlike the top of chip, the bottom (The opposite side of sapphire substrate) is the

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epitaxial Layer where the p-n junction is located. It is not mechanically protected and can be damaged if a sharp and hard ejector pin material is used.

- Seoul Viosys recommends an ejector pin with rounded edge to minimize the risk of mechanical damage.



(a) Sharp ejector pin tip may damage the Flip Chip (left). (b) A rounded tip minimizes the risk of damage caused by ejector pin (right).

*The above specifications are subject to change with prior notice.*

Seoul Viosys Co., Ltd  
NOV 10th, 2015