

Specification For Approval

Date: 2016/08/24

Page: 1 of 11

고객 승인원 관리대장

개정번호	개정일자	개정 Page	개정이력	담당자	비고
00	2016.01.15	-	신규제정 (가승인원)	장미나	
01	2016.03.15	4 Page	Maximum rating 개정, 전기 광학 특성 개정, 분류기준서 개정	장미나	
02	2016.03.23	7~9 page	분류기준서 개정	장미나	
03	2016.05.13	7~9 page	분류기준서 개정	류용우	
04	2016.06.09	7~9 page	분류기준서 개정	이금주	
05	2016.08.04	7~9 page	분류기준서 개정	류용우	
06	2016.08.24	7~9 page	분류기준서 개정	이금주	

Specification For Approval

Date: 2016/08/24

Page: 2 of 11

Customer: Seoul Semiconductor Co., Ltd**Part Name: A8070-3E**

Contents:

1. Features and Application
2. Part Name
3. Main Materials
4. Electrodes
5. Chip Diagram
6. Maximum Ratings
7. Typical Electro-Optical Characteristics at Ta=25°C
8. Mechanical Specifications
9. Visual Inspection
10. Sorting Bins and Product Name
11. Packing
12. Labeling
13. Precaution

Seoul Viosys Co., Ltd.		
Drawn by	Checked by	Approved by
K.J.LEE	-	K.W.KIM
16/08/24	-	16/08/24

Seoul Semiconductor Co., Ltd		
Checked by		Approved by

Specification For Approval

Date: 2016/08/24

Page: 3 of 11

1. Features and Application

High Luminous Intensity, Long Operation Life
Power Package Application

2. Part Name:

A8070-3E

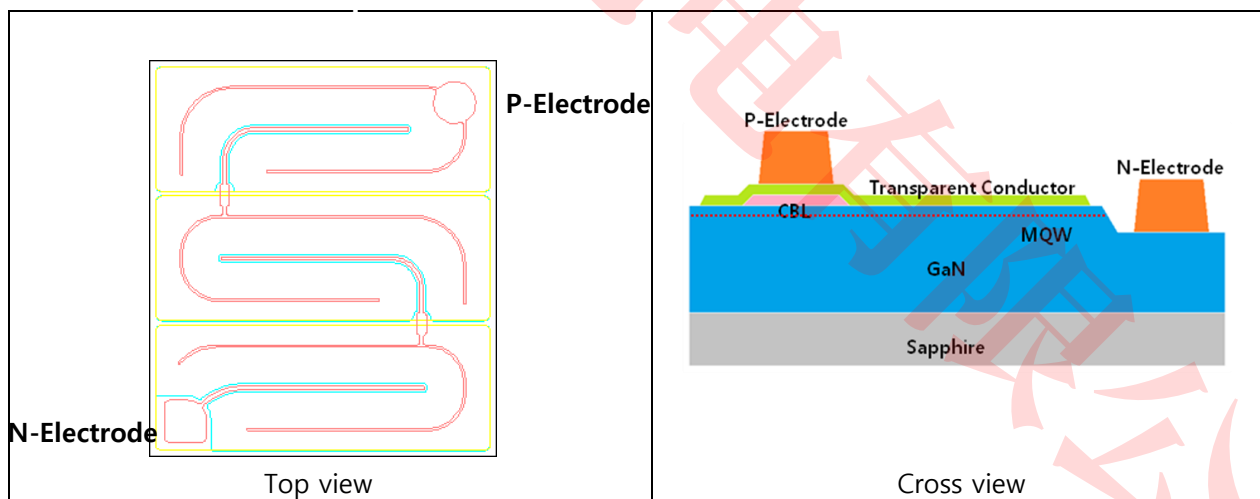
3. Main Material

Substrate: Al_2O_3 (Sapphire)
Epitaxial Layer: GaN for ESD

4. Electrodes

P-Electrode: Au alloy
N-Electrode: Au alloy

5. Chip Diagram



Specification For Approval

Date: 2016/08/24

Page: 4 of 11

6. Maximum Ratings

Item	Symbol	Value	Unit
DC forward current (Ta=25°C)	I _f	110	mA
Pulsed forward current ^a (Ta=25°C)	I _{fp}	130	mA
Junction temperature	T _j	125	°C
Operating temperature Range	T _{op}	-30 ~ +85	°C

^a1/10 Duty , f=1kHz

Note. 'Maximum Rating' described means that the chip has the possibility of breaking down when these conditions are exceeded momentarily. 'Maximum Rating' does not guarantee to use it continuously considering life under these conditions. 'Maximum Ratings' concerning your LED device after the chip is built into your package shall be established by yourself since these greatly depend on the design of the device, the conditions of assembly, the environment used, and so forth.

7. Typical Electro-Optical Characteristics at Ta=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn-on voltage	V _{F1}	I _f =100 μA	6.9	-	8.1	V
Forward voltage ^{a)}	V _{F2}	I _f =100mA	9.0	-	9.8	V
Dominant wavelength ^{b)}	λ _D	I _f =100mA	450	-	460	nm
Radiant power ^{c)}	P _o	I _f =100mA	450	-	610	mW

1. Radiant and Peak wavelength and voltage are measured by Seoul Viosys's equipment.

I_f: Forward Current

^aTolerance of measured Forward Voltage : ±3%

^bTolerance of measured Dominant Wavelength : ±1nm

^cTolerance of measured Radiant Power : ±10%

2. All chips are not getting measured ESD characteristics.

8. Mechanical Specifications

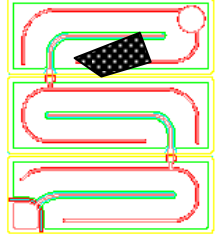
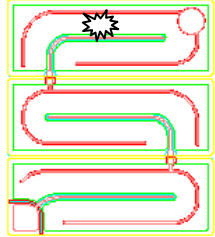
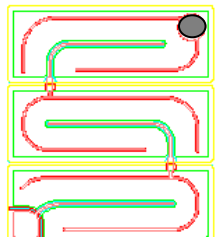
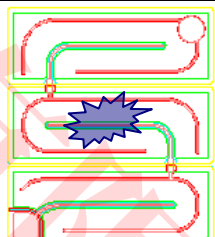
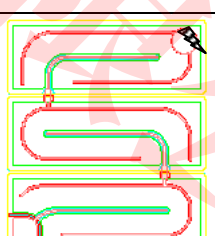
Description	Dimension (um)	Tolerance
Chip size	800x700	±10%
Chip thickness	150	±10um
p-pad diameter	85	±10um
n-pad diameter	85	±10um

Specification For Approval

Date: 2016/08/24

Page: 5 of 11

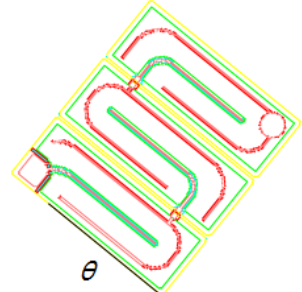
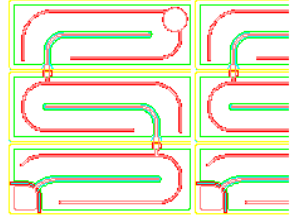
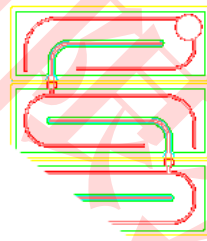
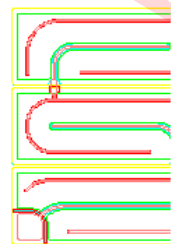
9. Visual inspection

Item	Accepted (OK) / Defective (NG)	Example
Surface dirt	accepted : if surface dirt(metal) less than 20% of unit cell.	
P-side TCL film peeling	accepted : if TCL film peeling less than 20% of unit cell.	
Partially missing bond pad	accepted : $a < b/5$ a: missing bond pad b: normal bond pad	
Back metal peeling	rejected : if Back Metal peeling more than 10% of chip area.	
Bond pad scratch	accepted : if bond pad scratch (including probe mark) less than 50 % of bond pad area	

Specification For Approval

Date: 2016/08/24

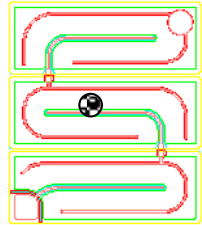
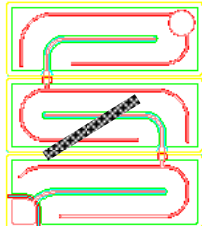
Page: 6 of 11

θ shift	accepted : $\theta < \pm 5^\circ$	
Twins or triples	Inseparable chips are rejected If extra-size is less than 10%, OK.	
Dicing shift	The light-emitting surface, pad can't be cut-off	
Chipping	Pad electrode not chipped off	
Bad cut	Not accepted : if bad cut is occurred	

Specification For Approval

Date: 2016/08/24

Page: 7 of 11

Pinholes	accepted : if pinhole less than 20% of unit cell	
Surface scratches	accepted : if surface scratch less than 20% of surface emitting area	

10. Sorting Bins and Product Name

Product Name (Rev.7)	BIN	Forward Voltage [V] @100uA	Forward Voltage [V] @100mA	Wavelength [nm] @100mA	Power [mW] @100mA
A8070-3E-Y01	1	6.9~8.1	9~9.4	450~452.5	450~460
A8070-3E-Y02	2	6.9~8.1	9~9.4	450~452.5	460~470
A8070-3E-Y03	3	6.9~8.1	9~9.4	450~452.5	470~490
A8070-3E-Y04	4	6.9~8.1	9~9.4	450~452.5	490~510
A8070-3E-Y05	5	6.9~8.1	9~9.4	450~452.5	510~530
A8070-3E-Y06	6	6.9~8.1	9~9.4	450~452.5	530~610
A8070-3E-Y07	7	6.9~8.1	9.4~9.6	450~452.5	450~460
A8070-3E-Y08	8	6.9~8.1	9.4~9.6	450~452.5	460~470
A8070-3E-Y09	9	6.9~8.1	9.4~9.6	450~452.5	470~490
A8070-3E-Y10	10	6.9~8.1	9.4~9.6	450~452.5	490~510
A8070-3E-Y11	11	6.9~8.1	9.4~9.6	450~452.5	510~530
A8070-3E-Y12	12	6.9~8.1	9.4~9.6	450~452.5	530~610
A8070-3E-Y13	13	6.9~8.1	9.6~9.8	450~452.5	450~460
A8070-3E-Y14	14	6.9~8.1	9.6~9.8	450~452.5	460~470
A8070-3E-Y15	15	6.9~8.1	9.6~9.8	450~452.5	470~490
A8070-3E-Y16	16	6.9~8.1	9.6~9.8	450~452.5	490~510
A8070-3E-Y17	17	6.9~8.1	9.6~9.8	450~452.5	510~530
A8070-3E-Y18	18	6.9~8.1	9.6~9.8	450~452.5	530~610
A8070-3E-Z01	19	6.9~8.1	9~9.4	452.5~455	450~460
A8070-3E-Z02	20	6.9~8.1	9~9.4	452.5~455	460~470
A8070-3E-Z03	21	6.9~8.1	9~9.4	452.5~455	470~490
A8070-3E-Z04	22	6.9~8.1	9~9.4	452.5~455	490~510
A8070-3E-Z05	23	6.9~8.1	9~9.4	452.5~455	510~530
A8070-3E-Z06	24	6.9~8.1	9~9.4	452.5~455	530~610

Specification For Approval

Date: 2016/08/24

Page: 8 of 11

A8070-3E-Z07	25	6.9~8.1	9.4~9.6	452.5~455	450~460
A8070-3E-Z08	26	6.9~8.1	9.4~9.6	452.5~455	460~470
A8070-3E-Z09	27	6.9~8.1	9.4~9.6	452.5~455	470~490
A8070-3E-Z10	28	6.9~8.1	9.4~9.6	452.5~455	490~510
A8070-3E-Z11	29	6.9~8.1	9.4~9.6	452.5~455	510~530
A8070-3E-Z12	30	6.9~8.1	9.4~9.6	452.5~455	530~610
A8070-3E-Z13	31	6.9~8.1	9.6~9.8	452.5~455	450~460
A8070-3E-Z14	32	6.9~8.1	9.6~9.8	452.5~455	460~470
A8070-3E-Z15	33	6.9~8.1	9.6~9.8	452.5~455	470~490
A8070-3E-Z16	34	6.9~8.1	9.6~9.8	452.5~455	490~510
A8070-3E-Z17	35	6.9~8.1	9.6~9.8	452.5~455	510~530
A8070-3E-Z18	36	6.9~8.1	9.6~9.8	452.5~455	530~610
A8070-3E-A01	37	6.9~8.1	9~9.4	455~457.5	450~460
A8070-3E-A02	38	6.9~8.1	9~9.4	455~457.5	460~470
A8070-3E-A03	39	6.9~8.1	9~9.4	455~457.5	470~490
A8070-3E-A04	40	6.9~8.1	9~9.4	455~457.5	490~510
A8070-3E-A05	41	6.9~8.1	9~9.4	455~457.5	510~530
A8070-3E-A06	42	6.9~8.1	9~9.4	455~457.5	530~610
A8070-3E-A07	43	6.9~8.1	9.4~9.6	455~457.5	450~460
A8070-3E-A08	44	6.9~8.1	9.4~9.6	455~457.5	460~470
A8070-3E-A09	45	6.9~8.1	9.4~9.6	455~457.5	470~490
A8070-3E-A10	46	6.9~8.1	9.4~9.6	455~457.5	490~510
A8070-3E-A11	47	6.9~8.1	9.4~9.6	455~457.5	510~530
A8070-3E-A12	48	6.9~8.1	9.4~9.6	455~457.5	530~610
A8070-3E-A13	49	6.9~8.1	9.6~9.8	455~457.5	450~460
A8070-3E-A14	50	6.9~8.1	9.6~9.8	455~457.5	460~470
A8070-3E-A15	51	6.9~8.1	9.6~9.8	455~457.5	470~490
A8070-3E-A16	52	6.9~8.1	9.6~9.8	455~457.5	490~510
A8070-3E-A17	53	6.9~8.1	9.6~9.8	455~457.5	510~530
A8070-3E-A18	54	6.9~8.1	9.6~9.8	455~457.5	530~610
A8070-3E-B01	55	6.9~8.1	9~9.4	457.5~460	450~460
A8070-3E-B02	56	6.9~8.1	9~9.4	457.5~460	460~470
A8070-3E-B03	57	6.9~8.1	9~9.4	457.5~460	470~490
A8070-3E-B04	58	6.9~8.1	9~9.4	457.5~460	490~510
A8070-3E-B05	59	6.9~8.1	9~9.4	457.5~460	510~530
A8070-3E-B06	60	6.9~8.1	9~9.4	457.5~460	530~610
A8070-3E-B07	61	6.9~8.1	9.4~9.6	457.5~460	450~460
A8070-3E-B08	62	6.9~8.1	9.4~9.6	457.5~460	460~470
A8070-3E-B09	63	6.9~8.1	9.4~9.6	457.5~460	470~490
A8070-3E-B10	64	6.9~8.1	9.4~9.6	457.5~460	490~510
A8070-3E-B11	65	6.9~8.1	9.4~9.6	457.5~460	510~530
A8070-3E-B12	66	6.9~8.1	9.4~9.6	457.5~460	530~610
A8070-3E-B13	67	6.9~8.1	9.6~9.8	457.5~460	450~460

Specification For Approval

Date: 2016/08/24

Page: 9 of 11

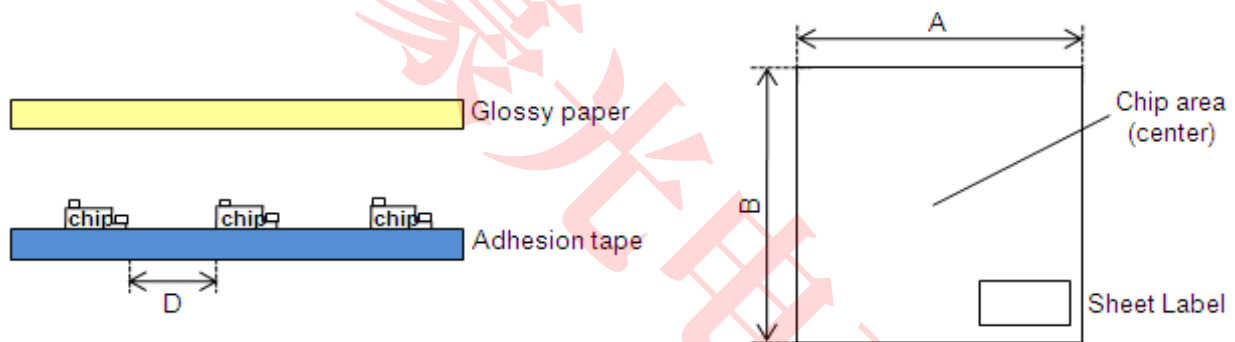
A8070-3E-B14	68	6.9~8.1	9.6~9.8	457.5~460	460~470
A8070-3E-B15	69	6.9~8.1	9.6~9.8	457.5~460	470~490
A8070-3E-B16	70	6.9~8.1	9.6~9.8	457.5~460	490~510
A8070-3E-B17	71	6.9~8.1	9.6~9.8	457.5~460	510~530
A8070-3E-B18	72	6.9~8.1	9.6~9.8	457.5~460	530~610

11. Packing

(1) Chips on tape

- (a) Electro-Optical measurement data should be labeled and tacked on the backside of the glossy paper. Chip area should be placed in the center of adhesion tape, and the wire-bonding pad should face towards the covered glossy paper.

(b)



- (b) Chip type, Lot No. and quantity etc. should be labeled and tacked to the corner of the glossy paper.

Item	Instruction
Adhesion tape	Semi- transparent blue
Glossy paper (A×B)	197mm × 220mm
Chip Qty tape	Typ. 5,600ea
Chip separation (D)	D : 0.2mm

(2) Packing for shipment

- (a) The sheets (adhesion tape + glossy paper) are packed in an anti-static electricity bag. Each anti-static bag can contain up to 20 sheets.

- (b) The anti-static bags are packed in a box. The size of this box is 250mm×65mm×275mm

(a) × (b) × (c). Each box can contain up to 5 anti-static electricity bags.

Specification For Approval

Date: 2016/08/24

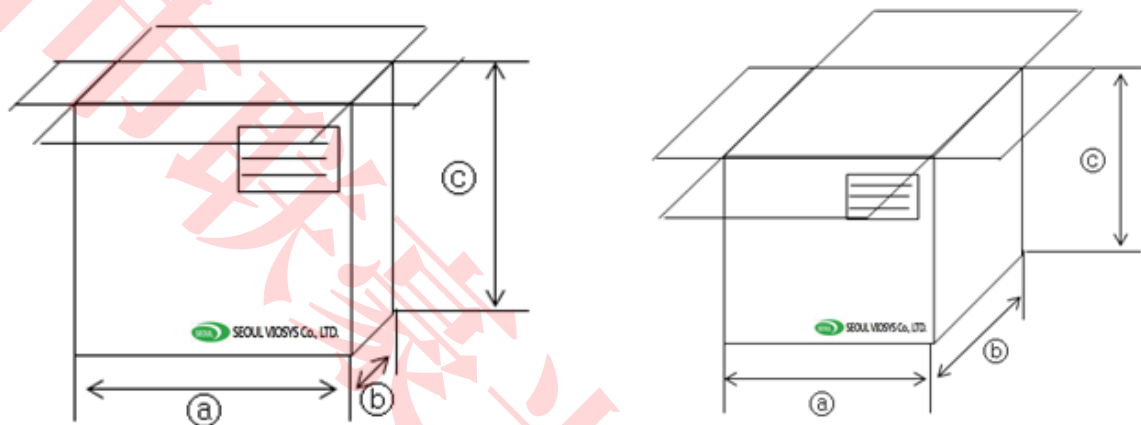
Page: 10 of 11

(c) The boxes which contain anti-static electricity bags are packed in the other box.

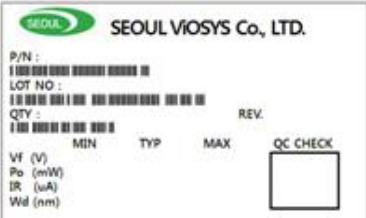
The size of this outer box is 260mm×340mm×290mm (a × b × c). Each outer box can contain up to 5 inner boxes.

(d) Each sheet / box is labeled with information describing its content.

(Details please refer to section 12)



10. Labeling

Sheet	Inner Box	Outer Box
		

(1) Sheet: The measurement data for each lot are also shown on the backside of the sheet.

(2) Inner Box: The information about the products is also shown on the inner box.

(3) Outer Box: The information about the products is also shown on the outer box

11. Precaution

(1) Quality Guarantee

The chip guarantee period is three months after the delivery under the following preservation conditions. If any defective is found, the customer shall immediately inform of that to Seoul Viosys Co., Ltd. Preservation conditions (when the shipping package is unopened.)

· Temperature: 0 ~ 60 °C

Specification For Approval

Date: 2016/08/24

Page: 11 of 11

- Atmosphere: Keep the chips in a desiccator with silica gel or with nitrogen substitution.
- (2) General precaution for use
 - Chips should be stored in a clean environment. If the Chips are to be stored for 3 months or more after being shipped from Seoul Viosys, they should be packed by a sealed container with nitrogen gas injected. (Shelf life of sealed bags: 1year, 0~40°C of temperature, 20~70% of RH)
 - This chip should not be used directly in any type of fluid such as water, oil, organic solvent, etc. When washing is required, IPA is recommended to use.
 - After storage bag is open, device subjected to soldering, solder flow, or other high temperature processes must be: Mounted within 168 hours (7days) at an assembly line with a condition of no more than 30°C and 60% RH
 - Chips require baking before mounting, if humidity card reading is >60% at, 23.5°C. Chips must be baked for 24Hrs. at 65.5°C, if baking required.
 - When the chips are illuminating, the maximum ambient temperature should be first considered before operation. If voltage exceeding the absolute maximum rating is applied to chips, it may cause damage or even destruction to chips. Damaged LEDs will show some abnormal characteristics such as remarkable increase of leak current, lower turn-on voltage and getting unlit at low current.
 - The appearance and specifications of the products may be modified for improvement without further notice.
 - The chips are sensitive to the static electricity and surge. It is strongly recommended to use a grounded wrist band and anti-electrostatic glove when handling the LEDs.

The above specifications are subject to change with prior notice.

Seoul Viosys Co., Ltd

AUG. 24th 2016