1B-25, 727, Wonsi-dong, Danwon-gu, Ansan-city, Gyeonggi-do, Korea 425-851

Specification for Approval	Date: 2015/09/07	Page : 1/9

Customer : Seoul Semiconductor Co., Ltd.

Part Name : PBS7221 I4C-E-L

Contents:

SEOUL VIOSYS Co., Ltd.		
Drawn by	Checked by	Approved by
D.-I. Suh	K.W. Kim	Y.J. Yoon
Sep 07th, 2015	Sep 07th, 2015	Sep 07th, 2015

Seoul Semiconductor Co., Ltd.		
Checked by		Approved by

1. Features and Applications

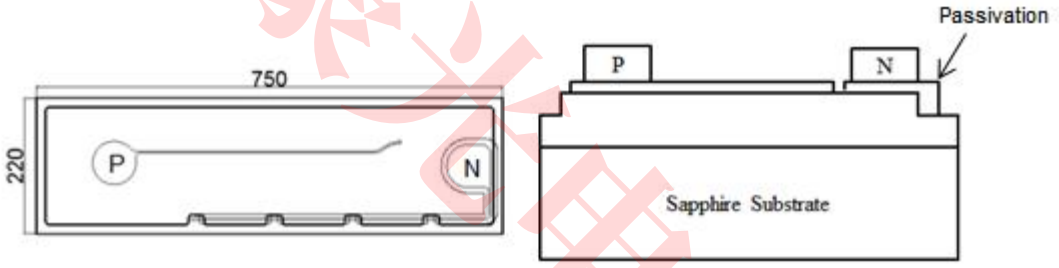
- High luminous intensity with long life.
- All Chips are 100% tested and sorted.
- Small & Medium LCD Backlighting and Lighting applications

2. Part Name : PBS7221 I4C-E-L

3. Main Material : InGaN/GaN on Sapphire

4. Electrodes : Anode - Au alloy ; Cathode - Au alloy

5. Chip Diagram



< Top-view > < Cross-view >

6. Maximum Ratings

Item	Symbol	Value	Unit
DC Forward Current (Ta=25℃)	I_F	80	mA
Pulsed Forward Current[a] (Ta=25℃)	I_{FP}	95	mA
Junction Temperature	T_J	100	℃
Operating Temperature	T_{op}	-30 ~ +85	℃
Temperature during Packaging	T_p	250 (<10sec)	℃

Note. 'Maximum Ratings' mean when it exceeds the chip has the possibility of breaking down when these conditions are exceeded momentarily. 'Maximum ratings' the chip is not guaranteed to endure such conditions. 'Maximum Ratings' concerning your LED device after the chip is built into your package shall be established by yourself since these greatly depend on the design of the device, the conditions of assembly, the environment used, and so forth.

[a] 1/10 Duty , f=1kHz

7. Typical Electro-Optical Characteristics at Ta=25℃

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reverse Current	I_R	V_R=5V	0		1.0	μA
Forward Voltage	V_{F1}	I_F=1μA	1.9		2.7	V
Forward Voltage	V_{F2}	I_F=20mA	2.7		3.1	V
Peak Wavelength[a]	λ_p	I_F=20mA	445		455	nm
Radiant Power[b]	Po	I_F=20mA	82			mW

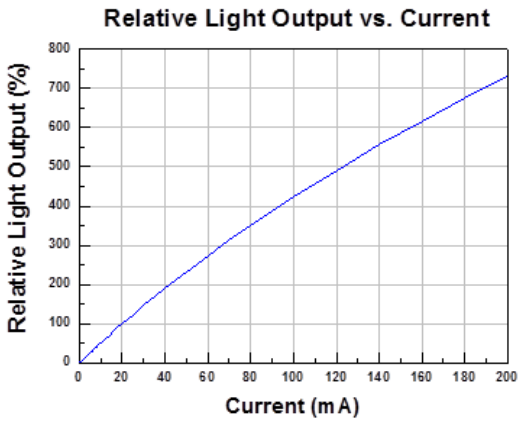
Note.

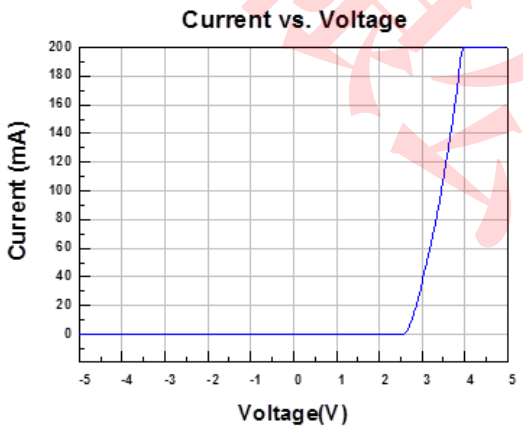
- All measurements are done with SEOUL VIOSYS' testing equipment.
- All Chips are 100% tested on ESD(HBM) and sorted.
- ESD protection is strongly recommended when handling chips.
- Reverse voltage is only applying for electrical characteristic measurement, any continuously reverse voltage applied to LED in not recommended and can cause metal migration.

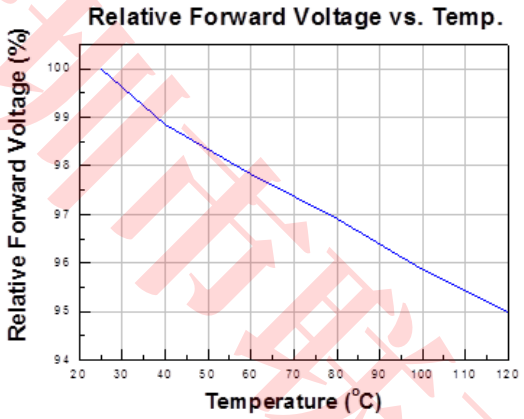
[a]Tolerance of measured wavelength : ±1nm

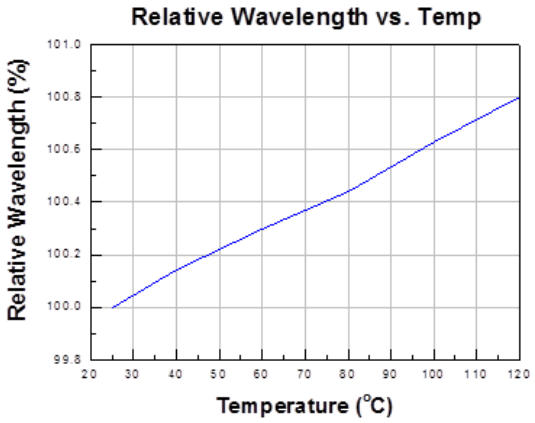
[b]Tolerance of measured Radiant power : ±10%

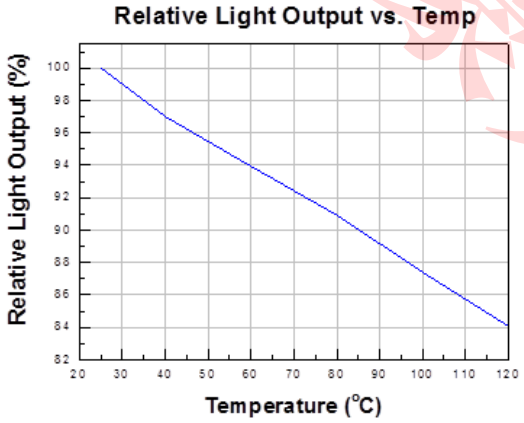
These following graphs represent typical performance of the **PBS7221 I4C-E-L** LED chip. Actual performance will vary slightly for different power and dominant wavelength bins.

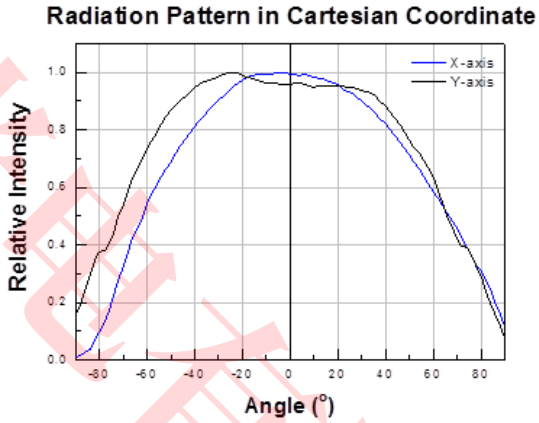








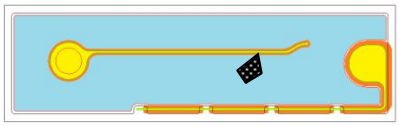
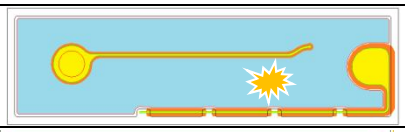
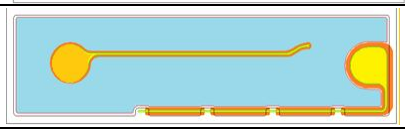
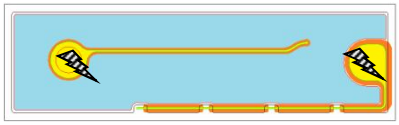
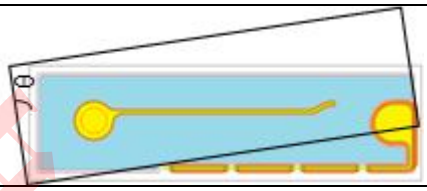
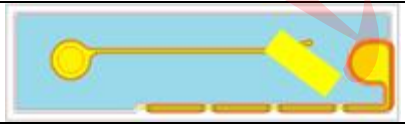


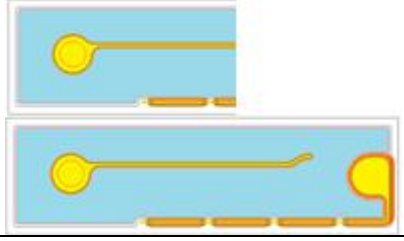


8. Mechanical Specifications

Description	Dimension (㎛)
Chip Size	220±30 x 750±40
Chip Thickness	140 ±10
P-Pad Diameter	70 ±5
N-PAD Diameter	70 ±5

9. Visual inspection

Item	NG criteria	NG Example
Surface contamination	Surface & Pad contamination larger than 10% of surface emitting area	
P-side TCO film peeling	ITO film peeling larger than 10% of surface emitting area	
Partially missing P(N)-bond pad	Bond pad area and connection metal area peeling	
Pad scratch	Scratches of pad (including second probing mark) larger than 50% pad area	
θ shift	θ Shift to be $\pm 5^{\circ}$	
Dicing shift & Chipping	MESA Line Broken or Touch	
Pinholes	Pinhole larger than 5% of surface emitting area	
Surface scratches	Surface scratch larger than 10% of surface emitting area	
Pad metal Residue	Surface pad metal residue larger than 10% of chip surface area	
Back EP Peeling	Back Reflective Metal Peeling occurred larger than 10% of substrate	

ESD Damage	ESD damaged chip	
Bad cut (Twins and triplets)	There should not be two or more per placement (Bad cut extrusion)	

10. Sorting Bins and Product Name

(1) Sorting Bins

I_R (uA)	V_{F1} (V)	V_{F2} (V)	λ_p (nm)		Po (mW)	
0 ~ 1.0	1.9 ~ 2.7	2.7 ~ 3.1	W	445 ~ 447.5	03	82 ~ 83
			X	447.5 ~ 450	11	83 ~ 84
			Y	450 ~ 452.5	04	84 ~ 85
			Z	452.5 ~ 455	12	85 ~ 86
					05	86 ~

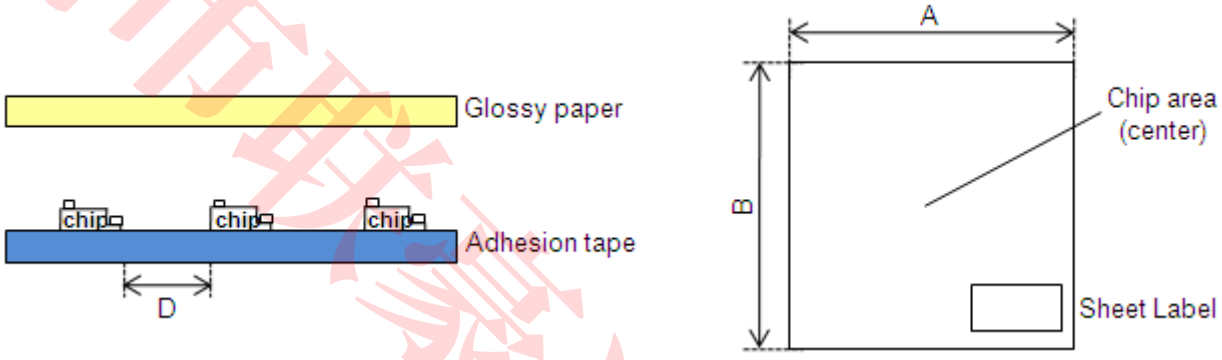
(2) Product Name (Rev10.)

Po (mW)	λ_p 445 - 447.5nm	λ_p 447.5 – 450nm	λ_p 450 - 452.5nm	λ_p 452.5 – 455nm	λ_p 455 – 457.5nm
79 - 80	PBS7221 I4C-E-L W01	PBS7221 I4C-E-L X01	PBS7221 I4C-E-L Y01	PBS7221 I4C-E-L Z01	
80 - 81	PBS7221 I4C-E-L W02	PBS7221 I4C-E-L X02	PBS7221 I4C-E-L Y02	PBS7221 I4C-E-L Z02	
81 - 82	PBS7221 I4C-E-L W10	PBS7221 I4C-E-L X10	PBS7221 I4C-E-L Y10	PBS7221 I4C-E-L Z10	
82 - 83	PBS7221 I4C-E-L W03	PBS7221 I4C-E-L X03	PBS7221 I4C-E-L Y03	PBS7221 I4C-E-L Z03	PBS7221 I4C-E-L A01
83 - 84	PBS7221 I4C-E-L W11	PBS7221 I4C-E-L X11	PBS7221 I4C-E-L Y11	PBS7221 I4C-E-L Z11	PBS7221 I4C-E-L A02
84 - 85	PBS7221 I4C-E-L W04	PBS7221 I4C-E-L X04	PBS7221 I4C-E-L Y04	PBS7221 I4C-E-L Z04	PBS7221 I4C-E-L A03
85 - 86	PBS7221 I4C-E-L W12	PBS7221 I4C-E-L X12	PBS7221 I4C-E-L Y12	PBS7221 I4C-E-L Z12	PBS7221 I4C-E-L A04
86 -	PBS7221 I4C-E-L W05	PBS7221 I4C-E-L X05	PBS7221 I4C-E-L Y05	PBS7221 I4C-E-L Z05	

11. Packing

(1) Chips on tape

(a) Electro-Optical measurement data should be labeled and tacked on the backside of the glossy paper. Chip area should be placed in the center of adhesion tape, and the wire-bonding pad should face towards the covered glossy paper.



(b) Chip type, Lot No. and quantity etc. should be labeled and tacked to the corner of the glossy paper.

Item	Instruction
Adhesion tape	Semi- transparent blue
Glossy paper (A×B)	195mm × 208mm
Chip Q'ty／tape	Min. 500ea Max. 15,000ea
Chip separation (D)	Typ. 0.18mm

(2) Packing for shipment

(a) The sheets (adhesion tape + glossy paper) are packed in an anti-static electricity bag.

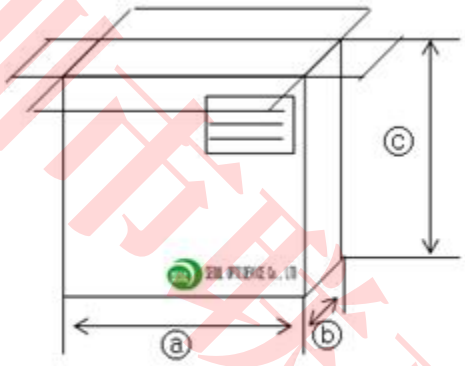
Each anti-static bag can contain up to 20 sheets.

(b) The anti-static bags are packed in a box. The size of this box is 250mm×65mm×275mm (ⓐ × ⓑ × ⓒ).

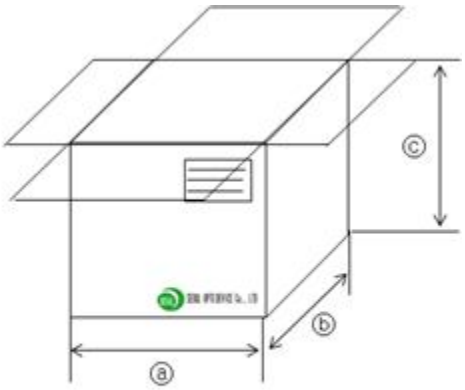
Each box can contain up to 5 anti-static electricity bags.

(c) The boxes which contain anti-static electricity bags are packed in the other box. The size of this outer box is 260mm×340mm×290mm (ⓐ × ⓑ × ⓒ). Each outer box can contain up to 5 inner boxes.

(d) Each sheet / box is labeled with information describing its content. (Details please refer to section 12)



< Inner box (b) >



< Outer box (c) >

12. Labeling

Sheet	Inner Box	Outer Box
SEOUL VIOSYS Co., LTD. P/N : LOT NO : QTY : REV. MIN TYP MAX QC CHECK Vf (V) Po (mW) IR (uA) Wd (nm)	LOT ID : XXXXXXXXX MODEL : XXXXXXXXX SHEET QTY : CHIP QTY :	LOT ID : XXXXXXXXX MODEL : XXXXXXXXX SHEET QTY : CHIP QTY :

(1) Sheet : The measurement data for each lot are also shown on the backside of the sheet.

(2) Inner Box : The information about the products is also shown on the inner box.

(3) Outer Box : The information about the products is also shown on the outer box.

13. Precaution

(1) Quality Guarantee

The chip guarantee period is three months after the delivery under the following preservation conditions. If any defective is found, the customer shall immediately inform of that to Seoul Viosys Co., Ltd.

Preservation conditions (when the shipping package is unopened.)

• Temperature : 0 ~ 60 °C

• Atmosphere : Keep the chips in a desiccator with silica gel or nitrogen substitution.

(2) Handling of Electrostatic Discharge

This product is designed to satisfy Human Body Model ESD. However these products are sensitive to static electricity charge and users are required to handle with care. If the applied current and/or voltage exceed the max rating, the overflow in energy may cause damage to, or possibly result in electrical destruction of the products.

Customer shall take absolutely secure countermeasure against static electricity and surge when handling products.

A protection device should be installed in the LED driving circuit, which does not exceed the maximum rating for surge current during on/ off switching. Proper grounding of products (via 1MΩ), use of conductive mat, semiconductive working uniform and shoes, and semiconductive containers are considered to be effective as countermeasures against static electricity and surge. It is recommended to use an ionizer in the facility or environment where static electricity may be generated easily.

(3) General precaution for use

Chips should be stored in a clean environment. If the Chips are to be stored for 3 months or more after being shipped from Seoul Viosys, they should be packed by a sealed container with nitrogen gas injected.

(Shelf life of sealed bags : 1year, 0~40°C of temperature , 20~70% of RH)

This chip should not be used directly in any type of fluid such as water, oil, organic solvent, etc. When washing is required, IPA is recommended to use.

After storage bag is open, device subjected to soldering, solder flow, or other high temperature processes must be:

Mounted within 168 hours (7days) at an assembly line with a condition of no more than 30°C and 60% RH

Chips require baking before mounting, if humidity card reading is >60% at, 23±5°C. chips must be baked for 24Hrs. at 65±5°C, if baking required.

When the chips are illuminating, the maximum ambient temperature should be first considered before operation. If voltage exceeding the absolute maximum rating is applied to chips, it may cause damage or even destruction to chips. Damaged LEDs will show some abnormal characteristics such as remarkable increase of leak current, lower turn-on voltage and getting unlit at low current.

The appearance and specifications of the products may be modified for improvement without further notice.

The chips are sensitive to the static electricity and surge. It is strongly recommended to use a grounded wrist band and anti-electrostatic glove when handling the LEDs.

The above specifications are subject to change with prior notice.

Seoul Viosys Co., Ltd.

Sep.07th , 2015