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Customer :

Part Name: Y1550-EB

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| Seoul Viosys Co., Ltd. | | |
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| Drawn by | Checked by | Approved by |
| 김재권 | 강민우 | 김종규 |

| Seoul Semiconductor Co., Ltd. | |
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1. Features and Application

- High Luminous Intensity, Long Operation Life
- Package-less module

2. Part Name:

- Y1550-EB

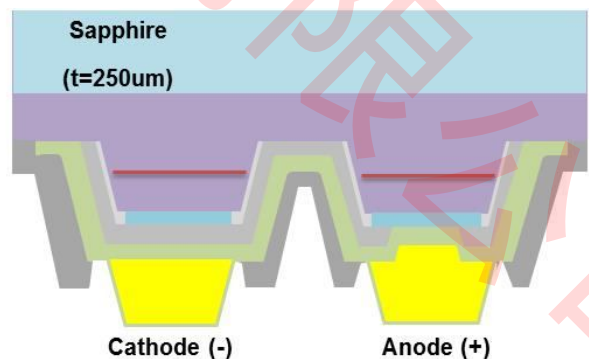
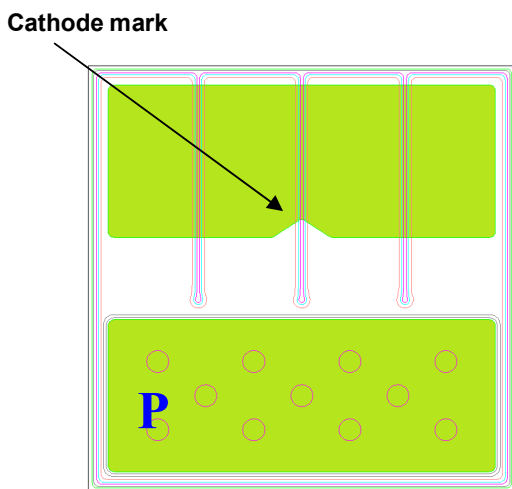
3. Main Material

- Substrate: Al₂O₃ (Sapphire)
- Epitaxial Layer: GaN Based LED Structure

4. Electrodes

- P-Electrode: Au alloy
- N-Electrode: Au alloy

5. Chip Diagram



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<Fig. 1> Plane View

<Fig. 2> Cross Sectional View

| Item | Symbol | Value | Unit |
|--|----------|-------------|------|
| DC forward current (Ta=25°C) | I_f | 1200 | mA |
| Pulsed forward current ^a (Ta=25°C) | I_{fp} | 1500 | mA |
| Junction temperature ^b | T_j | 125 | °C |
| Operating Temperature Range | T_{op} | -30 to + 85 | °C |
| Storage Temperature Range | T_{st} | -40 to +100 | °C |

6. Maximum Ratings

Note. 'Maximum Ratings' mean when it exceeds the chip has the possibility of breaking down when these conditions are exceeded momentarily. 'Maximum ratings', the chip is not guaranteed to endure such conditions. 'Maximum Ratings' concerning your LED device after the chip is built into your package shall be established by yourself since these greatly depend on the design of the device, the conditions of assembly, the environment used, and so forth.

^a 1/10 Duty , f=1kHz

^b Measurement condition ; Metal Core PCB

7. Typical Electro-Optical Characteristics at Ta=25°C

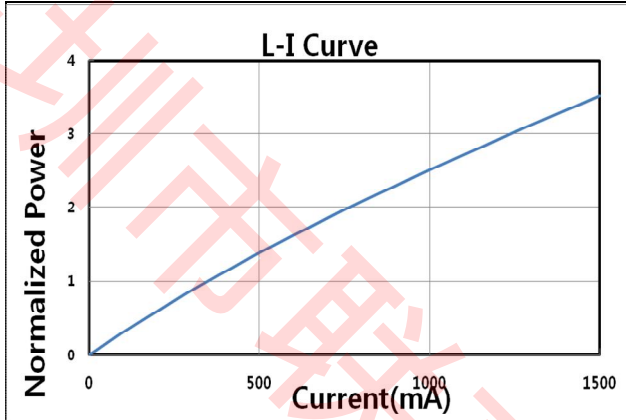
| Item | Symbol | Condition | Characteristics (Ta=25°C) | | | Unit |
|--|-----------------|-----------------|---------------------------|------|-------|------|
| | | | Min | Typ | Max | |
| Reverse Current | I_R | $V_R = -5V$ | 0 | - | 1.0 | uA |
| Turn-on Voltage | V_{F1} | $I_F = 1 \mu A$ | 1.8 | - | 2.7 | V |
| Forward Voltage | V_F | $I_F = 350mA$ | 2.70 | 2.90 | 3.10 | V |
| Dominant Wavelength ¹⁾ | λ_d | $I_F = 350mA$ | 450.0 | - | 460.0 | nm |
| Full Width Half Maximum | $\Delta\lambda$ | $I_F = 350mA$ | - | 30 | - | nm |
| Radiant Power ²⁾ | P_o | $I_F = 350mA$ | 490 | 525 | 570 | mW |

Note: Radiant and Dominant wavelength are measured by Seoul Viosys' equipment. (*1, *2)

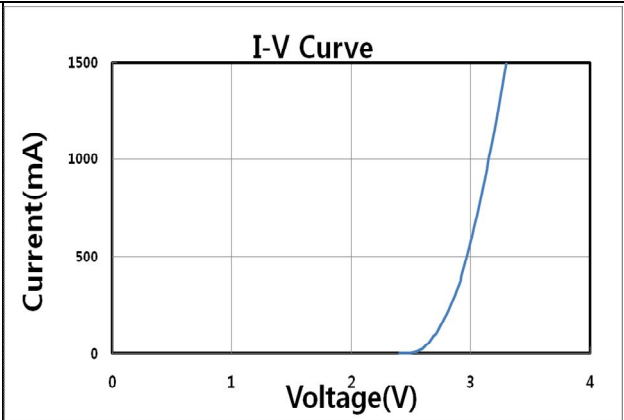
Dominant Wavelength: $\pm 1nm$. (*1)

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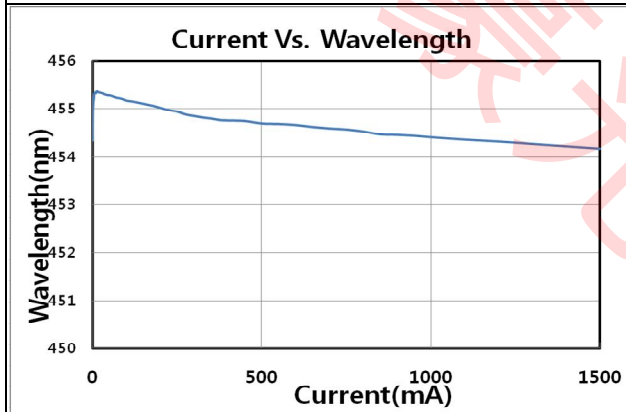
Radiant Power : $\pm 10\%$. (*2)



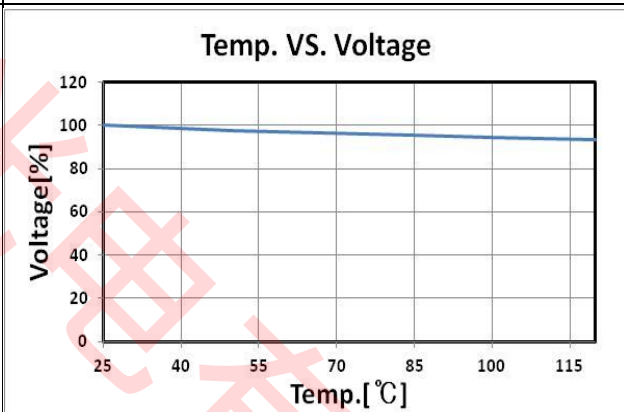
Forward Current vs. Light Output



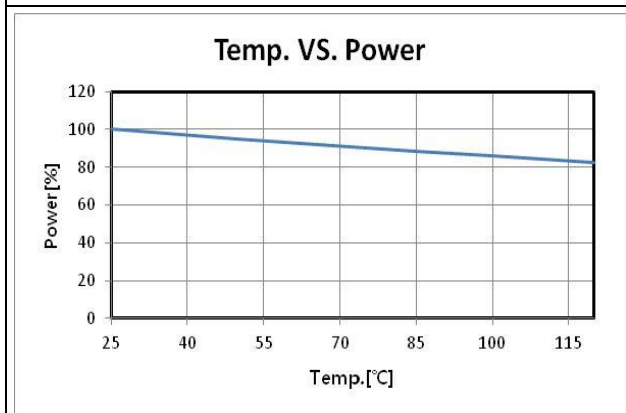
Forward Voltage vs. Forward Current



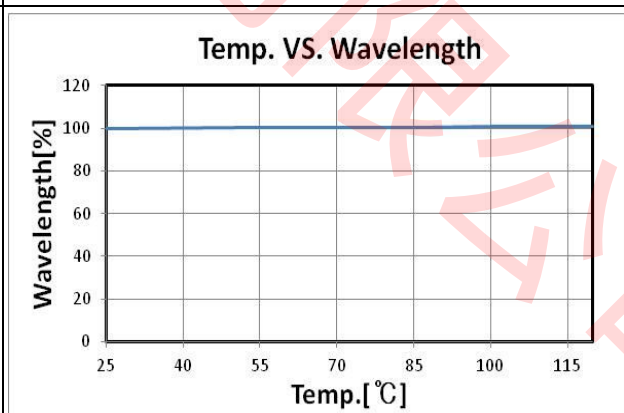
Forward Current vs. Wavelength



Temperature vs. Relative Forward Voltage



Temperature vs. Relative Light Output



Temperature vs. Relative Wavelength

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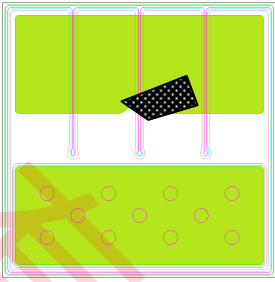
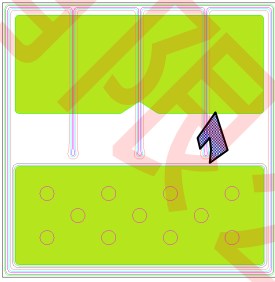
8. Mechanical Specifications

(Unit: μm)

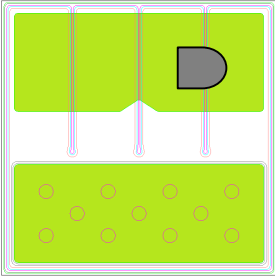
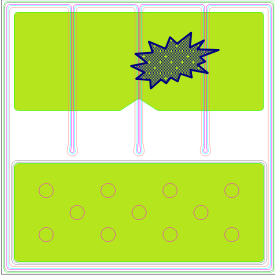
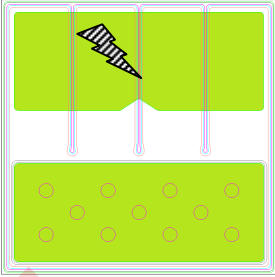
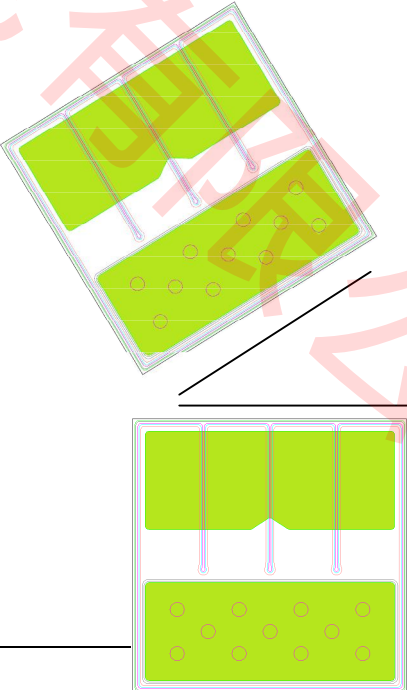
| Description | Dimension | Tolerance |
|-------------------|---|-----------|
| Top emitting area | 1550 μm x 1550 μm | ± 50 |
| Bottom substrate | 1550 μm x 1550 μm | ± 50 |
| Chip Thickness | 250 μm | ± 15 |
| P-Pad Diameter | 1410 μm x 555 μm | ± 50 |
| N-Pad Diameter | 1410 μm x 555 μm | ± 50 |

9. Visual inspection

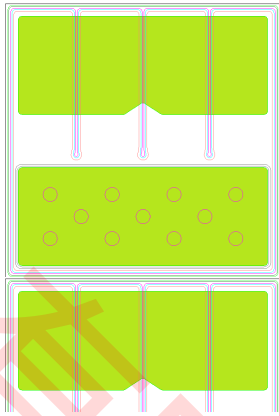
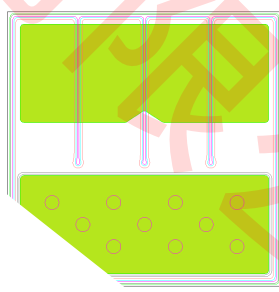
Done by microscope

| Item | Accepted (OK)/defective (N.G.) | Example |
|--------------------------|---|---|
| Surface dirt | accepted : if surface dirt(metal) less than 20% of chip |  |
| Passivation film peeling | accepted : if Passivation film peeling less than 30% of chip. |  |

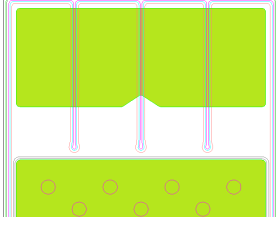
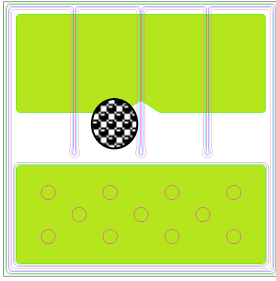
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| Partially missing pad | <p>accepted : $a < b/5$ a: missing bond pad b: normal bond pad</p> |  |
| Metal peeling | <p>rejected : if Metal peeling more than 20% of chip area.</p> |  |
| Bond pad scratch | <p>accepted : if bond pad scratch (including probe mark) less than 20 % of chip area.</p> |  |
| θ shift | <p>accepted : $\theta < \pm 5^\circ$</p> |  |

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| Twins or triples | Inseparable chips are rejected If extra-size is less than 10%, OK. |  |
| Chipping | Pad electrode not chipped off |  |

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| Bad cut | Not accepted : if bad cut is occurred |  |
| Pinholes | accepted : if pinhole less than 20% of chip |  |

10. Sorting Bins and Product name

| 제품명 | BIN | Reverse Leakage @-5V | Forward Voltage(V) @1uA | Forward Voltage(V) @ 350mA | Power(mW) @ 350mA | Wave Length(nm) @ 350mA |
|--------------|-----|----------------------|-------------------------|----------------------------|-------------------|-------------------------|
| Y1550-EB-Y01 | 1 | 0~1 | 1.8~2.7 | 2.7~2.98 | 490~495 | 450~452.5 |
| Y1550-EB-Y02 | 2 | 0~1 | 1.8~2.7 | 2.7~2.98 | 495~505 | 450~452.5 |
| Y1550-EB-Y03 | 3 | 0~1 | 1.8~2.7 | 2.7~2.98 | 505~520 | 450~452.5 |
| Y1550-EB-Y04 | 4 | 0~1 | 1.8~2.7 | 2.7~2.98 | 520~535 | 450~452.5 |
| Y1550-EB-Y05 | 5 | 0~1 | 1.8~2.7 | 2.7~2.98 | 535~550 | 450~452.5 |
| Y1550-EB-Y06 | 6 | 0~1 | 1.8~2.7 | 2.7~2.98 | 550~570 | 450~452.5 |
| Y1550-EB-Y07 | 7 | 0~1 | 1.8~2.7 | 2.98~3.1 | 490~495 | 450~452.5 |
| Y1550-EB-Y08 | 8 | 0~1 | 1.8~2.7 | 2.98~3.1 | 495~505 | 450~452.5 |
| Y1550-EB-Y09 | 9 | 0~1 | 1.8~2.7 | 2.98~3.1 | 505~520 | 450~452.5 |
| Y1550-EB-Y10 | 10 | 0~1 | 1.8~2.7 | 2.98~3.1 | 520~535 | 450~452.5 |
| Y1550-EB-Y11 | 11 | 0~1 | 1.8~2.7 | 2.98~3.1 | 535~550 | 450~452.5 |

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| Y1550-EB-Y12 | 12 | 0~1 | 1.8~2.7 | 2.98~3.1 | 550~570 | 450~452.5 |
| Y1550-EB-Z01 | 13 | 0~1 | 1.8~2.7 | 2.7~2.98 | 490~495 | 452.5~455 |
| Y1550-EB-Z02 | 14 | 0~1 | 1.8~2.7 | 2.7~2.98 | 495~505 | 452.5~455 |
| Y1550-EB-Z03 | 15 | 0~1 | 1.8~2.7 | 2.7~2.98 | 505~520 | 452.5~455 |
| Y1550-EB-Z04 | 16 | 0~1 | 1.8~2.7 | 2.7~2.98 | 520~535 | 452.5~455 |
| Y1550-EB-Z05 | 17 | 0~1 | 1.8~2.7 | 2.7~2.98 | 535~550 | 452.5~455 |
| Y1550-EB-Z06 | 18 | 0~1 | 1.8~2.7 | 2.7~2.98 | 550~570 | 452.5~455 |
| Y1550-EB-Z07 | 19 | 0~1 | 1.8~2.7 | 2.98~3.1 | 490~495 | 452.5~455 |
| Y1550-EB-Z08 | 20 | 0~1 | 1.8~2.7 | 2.98~3.1 | 495~505 | 452.5~455 |
| Y1550-EB-Z09 | 21 | 0~1 | 1.8~2.7 | 2.98~3.1 | 505~520 | 452.5~455 |
| Y1550-EB-Z10 | 22 | 0~1 | 1.8~2.7 | 2.98~3.1 | 520~535 | 452.5~455 |
| Y1550-EB-Z11 | 23 | 0~1 | 1.8~2.7 | 2.98~3.1 | 535~550 | 452.5~455 |
| Y1550-EB-Z12 | 24 | 0~1 | 1.8~2.7 | 2.98~3.1 | 550~570 | 452.5~455 |
| Y1550-EB-A01 | 25 | 0~1 | 1.8~2.7 | 2.7~2.98 | 490~495 | 455~457.5 |
| Y1550-EB-A02 | 26 | 0~1 | 1.8~2.7 | 2.7~2.98 | 495~505 | 455~457.5 |
| Y1550-EB-A03 | 27 | 0~1 | 1.8~2.7 | 2.7~2.98 | 505~520 | 455~457.5 |
| Y1550-EB-A04 | 28 | 0~1 | 1.8~2.7 | 2.7~2.98 | 520~535 | 455~457.5 |
| Y1550-EB-A05 | 29 | 0~1 | 1.8~2.7 | 2.7~2.98 | 535~550 | 455~457.5 |
| Y1550-EB-A06 | 30 | 0~1 | 1.8~2.7 | 2.7~2.98 | 550~570 | 455~457.5 |
| Y1550-EB-A07 | 31 | 0~1 | 1.8~2.7 | 2.98~3.1 | 490~495 | 455~457.5 |
| Y1550-EB-A08 | 32 | 0~1 | 1.8~2.7 | 2.98~3.1 | 495~505 | 455~457.5 |
| Y1550-EB-A09 | 33 | 0~1 | 1.8~2.7 | 2.98~3.1 | 505~520 | 455~457.5 |
| Y1550-EB-A10 | 34 | 0~1 | 1.8~2.7 | 2.98~3.1 | 520~535 | 455~457.5 |
| Y1550-EB-A11 | 35 | 0~1 | 1.8~2.7 | 2.98~3.1 | 535~550 | 455~457.5 |
| Y1550-EB-A12 | 36 | 0~1 | 1.8~2.7 | 2.98~3.1 | 550~570 | 455~457.5 |
| Y1550-EB-B01 | 37 | 0~1 | 1.8~2.7 | 2.7~2.98 | 490~495 | 457.5~460 |
| Y1550-EB-B02 | 38 | 0~1 | 1.8~2.7 | 2.7~2.98 | 495~505 | 457.5~460 |
| Y1550-EB-B03 | 39 | 0~1 | 1.8~2.7 | 2.7~2.98 | 505~520 | 457.5~460 |
| Y1550-EB-B04 | 40 | 0~1 | 1.8~2.7 | 2.7~2.98 | 520~535 | 457.5~460 |
| Y1550-EB-B05 | 41 | 0~1 | 1.8~2.7 | 2.7~2.98 | 535~550 | 457.5~460 |
| Y1550-EB-B06 | 42 | 0~1 | 1.8~2.7 | 2.7~2.98 | 550~570 | 457.5~460 |
| Y1550-EB-B07 | 43 | 0~1 | 1.8~2.7 | 2.98~3.1 | 490~495 | 457.5~460 |

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|--------------|----|-----|---------|----------|---------|-----------|
| Y1550-EB-B08 | 44 | 0~1 | 1.8~2.7 | 2.98~3.1 | 495~505 | 457.5~460 |
| Y1550-EB-B09 | 45 | 0~1 | 1.8~2.7 | 2.98~3.1 | 505~520 | 457.5~460 |
| Y1550-EB-B10 | 46 | 0~1 | 1.8~2.7 | 2.98~3.1 | 520~535 | 457.5~460 |
| Y1550-EB-B11 | 47 | 0~1 | 1.8~2.7 | 2.98~3.1 | 535~550 | 457.5~460 |
| Y1550-EB-B12 | 48 | 0~1 | 1.8~2.7 | 2.98~3.1 | 550~570 | 457.5~460 |

11. Packing

(1) Chips on tape

- (a) Electro-Optical measurement data should be labeled and tacked on the backside of the glossy paper. Chip area should be placed in the center of adhesion tape, and the wire-bonding pad should face towards the covered glossy paper.



- (b) Chip type, Lot No. and quantity etc. should be labeled and tacked to the corner of the glossy paper.

| Item | Instruction |
|---------------------|------------------------|
| Adhesion tape | Semi- transparent blue |
| Glossy paper (A×B) | 197mm × 220mm |
| Chip Qty tape | Typ. 1,190ea |
| Chip separation (D) | D : 0.40mm |

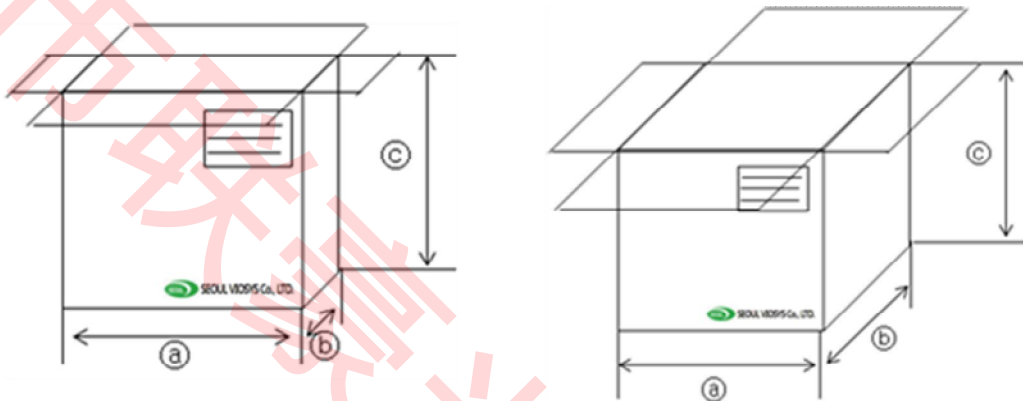
(2) Packing for shipment

- (a) The sheets (adhesion tape + glossy paper) are packed in an anti-static electricity bag. Each anti-static bag can contain up to 20 sheets.
- (b) The anti-static bags are packed in a box. The size of this box is 250mm×65mm×275mm (a × b × c). Each box can contain up to 5 anti-static electricity bags.
- (c) The boxes which contain anti-static electricity bags are packed in the other box. The size of this outer box is 260mm×340mm×290mm (a × b × c). Each outer box can

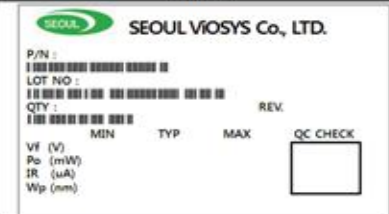


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contain up to 5 inner boxes.

(d) Each sheet / box is labeled with information describing its content. (Details please refer to section 12)



12. Labeling

| Sheet | Inner Box | Outer Box |
|---|---|---|
|  |  |  |

- (1) Sheet : The measurement data for each lot are also shown on the backside of the sheet.
- (2) Inner Box : The information about the products is also shown on the inner box.
- (3) Outer Box : The information about the products is also shown on the outer box.

13. Precaution

- (1) Quality Guarantee

The chip guarantee period is three months after the delivery under the following preservation conditions. If any defective is found, the customer shall immediately inform of

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that to Seoul Viosys Co., Ltd. Preservation conditions (when the shipping package is unopened.)

- Temperature: 0 ~ 60 °C
- Atmosphere: Keep the chips in a desiccator with silica gel or with nitrogen substitution.

(2) General precautions for use

- Chips should be stored in a clean environment. If the Chips are to be stored for 3 months or more after being shipped from Seoul Viosys, they should be packed by a sealed container with nitrogen gas injected.

(Shelf life of sealed bags : 1year, 0~40°C of temperature , 20~70% of RH)

- This chip should not be used directly in any type of fluid such as water, oil, organic solvent, etc. When washing is required, IPA is recommended to use.

- After storage bag is open, device subjected to soldering, solder flow, or other high temperature processes must be:

Mounted within 168 hours (7days) at an assembly line with a condition of no more than 30°C and 60% RH

- Chips require baking before mounting, if humidity card reading is >60% at, 23.5°C. chips must be baked for 24Hrs. at 65.5°C, if baking required.

- When the chips are illuminating, the maximum ambient temperature should be first considered before operation. If voltage exceeding the absolute maximum rating is applied to chips, it may cause damage or even destruction to chips. Damaged LEDs will show some abnormal characteristics such as remarkable increase of leak current, lower turn-on voltage and getting unlit at low current.

- The appearance and specifications of the products may be modified for improvement without further notice.

- The chips are sensitive to the static electricity and surge. It is strongly recommended to use a grounded wrist band and anti-electrostatic glove when handling the LEDs.

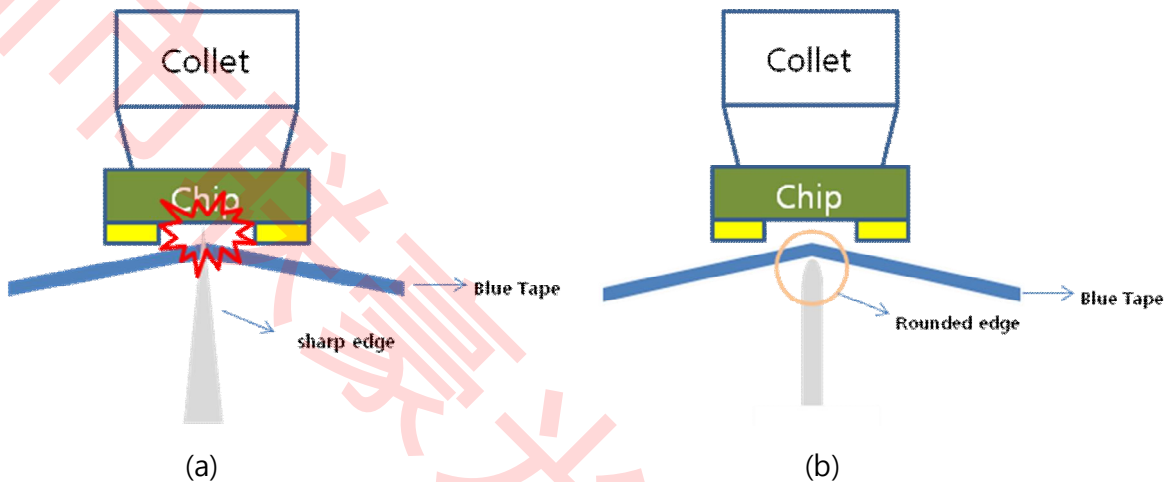
(3) Precautions for Die Attach (Pick and Place)

- Unlike the top of chip, the bottom (The opposite side of sapphire substrate) is the

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epitaxial Layer where the p-n junction is located. It is not mechanically protected and can be damaged if a sharp and hard ejector pin material is used.

- Seoul Viosys recommends an ejector pin with rounded edge to minimize the risk of mechanical damage.



(a) Sharp ejector pin tip may damage the Flip Chip (left). (b) A rounded tip minimizes the risk of damage caused by ejector pin (right).

The above specifications are subject to change with prior notice.

Seoul Viosys Co., Ltd
JUL 21th, 2016