1B-25, 727, Wonsi-dong, Danwon-gu, Ansan-city, Gyeonggi-do, Korea 425-851

고객 승인원 관리대장

개정번호	개정일자	개정 Page	개정이력	담당자	비고
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1B-25, 727, Wonsi-dong, Danwon-gu, Ansan-city, Gyeonggi-do, Korea 425-851

Customer: Seoul Semiconductor Co., Ltd

Part Name: A8070-6E

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Seoul Viosys Co., Ltd.		
Drawn by	Checked by	Approved by
M.N.JANG	K.J.LEE	K.W.KIM
16/12/13	16/12/13	16/12/13

Seoul Semiconductor Co., Ltd		
Checked by		Approved by

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1. Features and Application

High Luminous Intensity

Design for high voltage operation

Lighting alliances applications

2. Part Name:

A8070-6E

3. Main Material

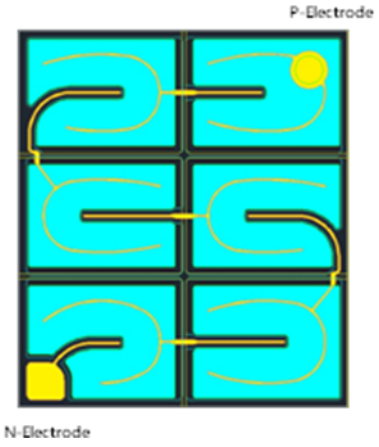
InGaN/GaN on Sapphire

4. Electrodes

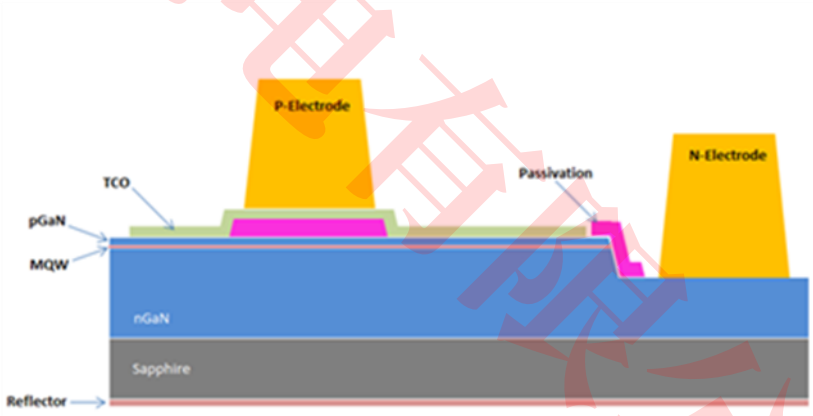
P-Electrode: Au

N-Electrode: Au

5. Chip Diagram



< Top view >



< Cross view >

6. Maximum Ratings

Item	Symbol	Value	Unit
DC forward current (Ta=25℃)	I_f	60	mA
Pulsed forward current [a] (Ta=25℃)	I_{fp}	70	mA
Junction temperature	T_j	125	℃
Operating temperature Range	T_{op}	-30 ~ +85	℃
Temperature during packaging	T_p	250 (<10sec)	℃

Note. 'Maximum Rating' described means that the chip has the possibility of breaking down when these conditions are exceeded momentarily. 'Maximum Rating' does not guarantee to use it continuously considering life under these conditions. 'Maximum Ratings' concerning your LED device after the chip is built into your package shall be established by yourself since these greatly depend on the design of the device, the conditions of assembly, the environment used, and so forth.

7. Typical Electro-Optical Characteristics at Ta=25℃

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn-on voltage	V_{F1}	I_F =100 μA	13.8	-	16.2	V
Forward voltage[a)]	V_{F2}	I_F =50mA	17.8	-	19.6	V
Dominant wavelength[b)]	λ_D	I_F =50mA	450	-	460	nm
Radiant power[c)]	Po	I_F =50mA	460	-	700	mW

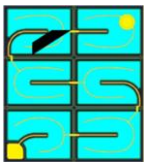
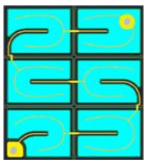
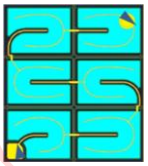
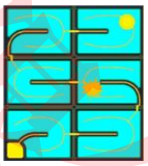
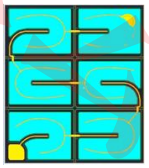
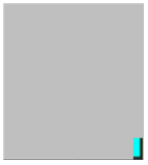
- Radiant and Peak wavelength and voltage are measured by Seoul Viosys's equipment.
- Electrostatic Discharge (ESD) protection epitaxy layer is applied.
- Electrostatic Discharge (ESD) protection is strongly recommended when handling chips

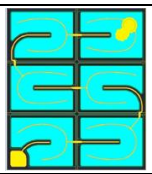
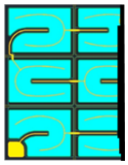
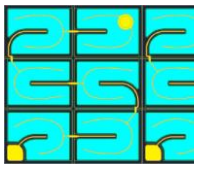
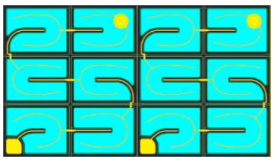
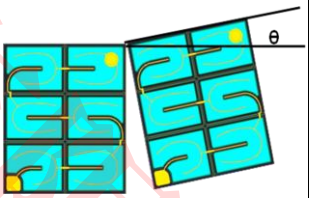
I_F: Forward Current
[a]Tolerance of measured Forward Voltage : ±3%
[b]Tolerance of measured Dominant Wavelength : ±1nm
[c]Tolerance of measured Radiant Power : ±10%

8. Mechanical Specifications

Description	Dimension (um)	Tolerance
Chip size	800x700	±10%
Chip thickness	180	±10um
p-pad diameter	80	±10um
n-pad diameter	80	±10um

9. Visual inspection

Item	NG criteria	NG Example
Pinhole	Larger than 5% of surface emitting area	
Surface contamination	Surface contamination Larger than 10% of surface emitting area	
Pad contamination	Pad contamination Larger than quarter of pad bonding area	
Surface scratches	Larger than 10% of surface emitting area	
Pad scratch	Larger than 50% of pad area (Including probing mark)	
TCL film peeling	Larger than 10% of surface emitting area	
Partially missing P/N Pad	Larger than 10% of bond pad area Larger than 2/3 of finger pad area	
Back metal Peeling	Larger than 10% of chip area	

Pad metal Residue	Larger than 10% of chip surface area	
Dicing shift	The light-emitting surface, N-pad and P-pad can't be cut-off	
Chipping	N-Pad, P-Pad or TC line chipped off	
Bad cut	Extrusion √ Out of chip size tolerance √ Including the pad metal of other chips	
Twins or triplets	Inseparable chips	
θ shift	θ > ±5° (10°)	

10. Sorting Bins and Product Name (Rev.4)

(1) Sorting Bins

V_{F1} (V)	V_{F2} (V)	λ_D (nm)	Po (mW)
13.8~16.2	17.8~18.4	450~452.5	470~480
	18.4~19		480~500
	19~19.6		500~520
			520~540
			540~700

V_{F1} (V)	V_{F2} (V)	λ_D (nm)	Po (mW)
13.8~16.2	17.8~18.4	452.5~455	460~480
	18.4~19	455~457.5	480~500
	19~19.6	457.5~460	500~520
			520~540
			540~700

(2) Product Name: A8070-6E-*1*2*3*4

*1*2*3	*1*2*3			
	450~452.5nm	452.5~455nm	455~457.5nm	457.5~460nm
460~480	-	Z46	A46	B46
470~480	Y47	-	-	-
480~500	Y48	Z48	A48	B48
500~520	Y50	Z50	A50	B50
520~540	Y52	Z52	A52	B52
540~700	Y54	Z54	A54	B54

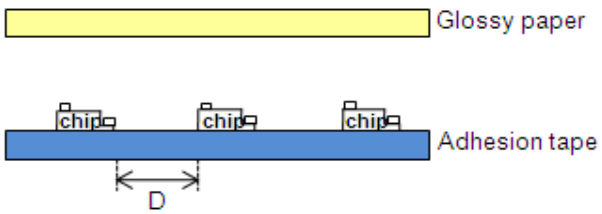
*4	17.8~18.4	18.4~19	19~19.6
Grade	L	M	H

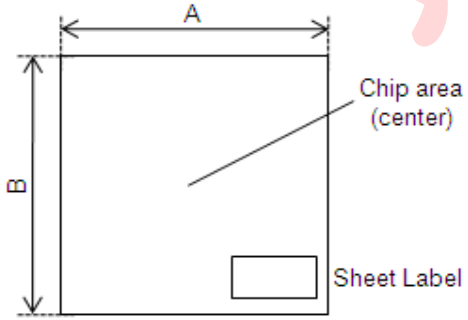
11. Packing

(1) Chips on tape

(a) Electro-Optical measurement data should be labeled and tacked on the backside of the glossy paper. Chip area should be placed in the center of adhesion tape, and the wire-bonding pad should face towards the covered glossy paper.

(b)





(b) Chip type, Lot No. and quantity etc. should be labeled and tacked to the corner of the glossy paper.

Item	Instruction
Adhesion tape	Semi- transparent blue
Glossy paper (A×B)	197mm × 220mm
Chip Qty tape	Typ. 6,200ea
Chip separation (D)	D : 0.2mm

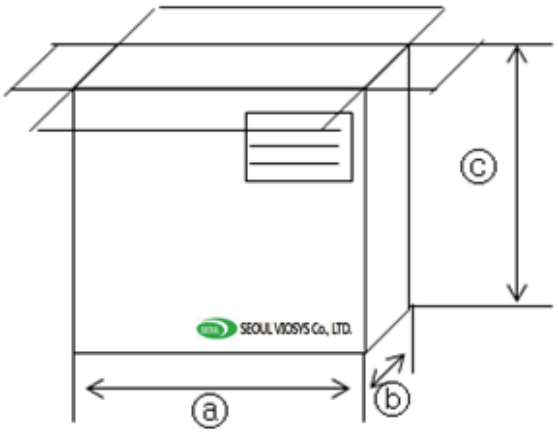
(2) Packing for shipment

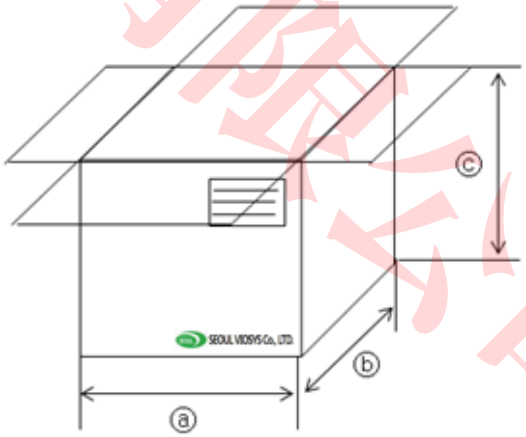
(a) The sheets (adhesion tape + glossy paper) are packed in an anti-static electricity bag. Each anti-static bag can contain up to 20 sheets.

(b) The anti-static bags are packed in a box. The size of this box is 250mm×65mm×275mm (ⓐ × ⓑ × ⓒ). Each box can contain up to 5 anti-static electricity bags.

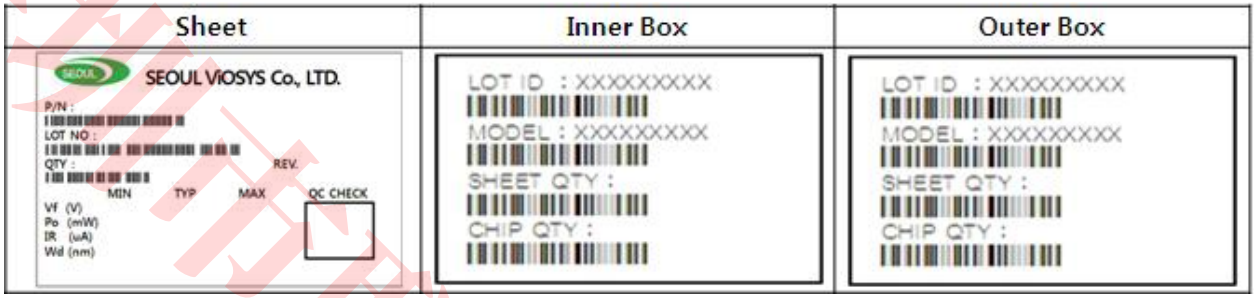
(c) The boxes which contain anti-static electricity bags are packed in the other box.
The size of this outer box is 260mm×340mm×290mm (ⓐ × ⓑ × ⓒ). Each outer box can contain up to 5 inner boxes.

(d) Each sheet / box is labeled with information describing its content. (Details please refer to section 11)





12. Labeling



(1) Sheet: The measurement data for each lot are also shown on the backside of the sheet.

(2) Inner Box: The information about the products is also shown on the inner box.

(3) Outer Box: The information about the products is also shown on the outer box

13. Precaution

(1) Quality Guarantee

The chip guarantee period is three months after the delivery under the following preservation conditions. If any defective is found, the customer shall immediately inform of that to Seoul Viosys Co., Ltd. Preservation conditions (when the shipping package is unopened.)

· Temperature: 0 ~ 60 ˚C

· Atmosphere: Keep the chips in a desiccator with silica gel or with nitrogen substitution.

(2) General precaution for use

· Chips should be stored in a clean environment. If the Chips are to be stored for 3 months or more after being shipped from Seoul Viosys, they should be packed by a sealed container with nitrogen gas injected. (Shelf life of sealed bags: 1year, 0~40˚C of temperature, 20~70% of RH)

· This chip should not be used directly in any type of fluid such as water, oil, organic solvent, etc. When washing is required, IPA is recommended to use.

· After storage bag is open, device subjected to soldering, solder flow, or other high temperature processes must be: Mounted within 168 hours (7days) at an assembly line with a condition of no more than 30˚C and 60% RH

· Chips require baking before mounting, if humidity card reading is >60% at, 23.5˚C. Chips must be baked for 24Hrs. at 65.5˚C, if baking required.

· When the chips are illuminating, the maximum ambient temperature should be first considered

before operation. If voltage exceeding the absolute maximum rating is applied to chips, it may cause damage or even destruction to chips. Damaged LEDs will show some abnormal characteristics such as remarkable increase of leak current, lower turn-on voltage and getting unlit at low current.

· The appearance and specifications of the products may be modified for improvement without further notice.

· The chips are sensitive to the static electricity and surge. It is strongly recommended to use a grounded wrist band and anti-electrostatic glove when handling the LEDs.

The above specifications are subject to change with prior notice.

Seoul Viosys Co., Ltd

DEC 13th 2016